2026 IEEE Radio Frequency Integrated Circuits Symposium

Boston, Massachusetts, USA
7–9 June 2026

RFIC

IEEE

PROGRAM

Sponsored by

IEEE Microwave Theory and Technology Society
IEEE Electron Devices Society
and
IEEE Solid-State Circuits Society

MTT-S IEEE MICROWAVE THEORY & TECHNOLOGY SOCIETY

EDS ELECTRON DEVICES SOCIETY

SSCS IEEE Solid-State Circuits Society

RFIC Plenary, Reception, and Symposium Showcase

Sunday Evening, 7 June 2026
Thomas M. Menino Convention & Exhibition Center (MCEC)
& Westin Boston Seaport District (Westin)

Enjoy an entertaining and relaxing evening with your RFIC colleagues and friends at the special Sunday night RFIC events.

17:30–19:00, Plenary Session, MCEC Ballroom: The evening begins with a warm welcome by the General Chair and the TPC Chair, the Student Paper Awards, the Industry Paper Awards, and the Tina Quach Service Award ceremony followed by two plenary speakers: Prof. Asad Abidi from UCLA, and Dr. Oliver Dial from IBM.

19:30–21:00, RFIC Reception and Symposium Showcase, Westin Grand Ballroom: Food and drinks will be provided while you connect with colleagues, friends, make new acquaintances, and catch up on the latest developments in the field. The Symposium Showcase will feature our industry and student paper awards finalists. The selected authors will present their innovative work in electronic poster format.

Your admittance is included with the RFIC Symposium registration and the Super-pass registration. Those who cannot attend the rest of RFIC but don't want to miss the event can purchase Sunday-night-only tickets. Please see https://rfic-ieee.org/ for more details.

The RFIC Symposium is made possible through the generous support of our corporate sponsors:

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RFIC Symposium Schedule (6–9 June 2026)

Event	Location	Sat 6 June	Sun 7 June	Mon 8 June	Tue 9 June
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Speakers' Breakfast	258ABC			07:00–08:00	
Workshops	Sun: 151AB, 152, 153AB, 153C, 154, 156AB, 156C, 157AB, 157C, 158, 252AB, 254AB, 255, 256, 257AB Mon: 157C		08:00–11:30 13:30–17:20	08:00–11:50	
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Technical Lecture	253ABC		11:45–13:15		
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Reception and Symposium Showcase	Westin, Grand Ballroom		19:30–21:00		
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Panel Session	253ABC			12:00–13:20	
Student-Industry-Academia RFIChat	259AB				17:30–19:00

Westin: Westin Boston Seaport District

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Welcome Message from Chairs

Join us at the IEEE Radio Frequency Integrated Circuits Symposium (RFIC)—the premier global event celebrating innovation and excellence in radio frequency, millimeter-wave, and wireless integrated circuits. More than just a symposium, RFIC is where our community gathers to learn, connect, and lead. Experience inspiring keynotes from world-class educators, thought-provoking technical sessions, and lively networking with industry leaders. You can also participate in interactive panels and special student events designed to spark new ideas and shape the future of the field.

The event will be held at the Boston Convention Center from Sunday 7 June through Tuesday 9 June. Building on the strong momentum from last year, the RFIC 2026 technical program continues to prioritize quality and growth. We are maintaining the conditional acceptance process, which has successfully expanded the program while enhancing paper quality. Additionally, we are retaining the highly effective industry track to ensure we attract top-tier papers from across the industry.

Technical sessions will cover a comprehensive range of topics, from foundational areas like wireless SoCs, power amplifiers, and frequency synthesizers to advanced packaging and testing technologies. We are also featuring cutting-edge emerging topics, such as AI for RF circuits, D-band, quantum computing, and optical circuits. Furthermore, the program will showcase system-level innovations across imaging, satellite communications, and biomedical fields.

The symposium begins on Sunday with a comprehensive slate of RFIC-focused workshops covering a wide range of advanced topics:

- Frequency Generation: RF to sub-terahertz frequency synthesis.
- Wireless and Beamforming: Next-gen defense, commercial beamforming, and 6G multi-beam array architectures.
- Front-Ends and Amplifiers: Broadband, power-efficient front-ends, high-bandwidth interfaces (optical/wireless), FR3 Power Amplifiers, and low-power/batteryless radios.
- High-Frequency and Specialized Systems: D-Band (above 100 GHz) and G-Band circuits for communication and sensing, SpaceCom RFICs for harsh environments, and next-frontier radar systems.

Building on the success of last year's Technical Lecture , this year's program presents a 90-minute lecture on Sunday by Prof. Bram Nauta of the University of Twente, the Netherlands. He will explore how passive mixers are utilized in modern receivers to achieve excellent linearity and narrow-band RF filtering. This filtering is achieved by exploiting the mixer in an N-path filter configuration—a technique revived from forgotten times to solve modern challenges.

The RFIC Plenary Session will be a major highlight, featuring conference updates, the presentation of the Student and Industry Best Paper Awards, and two distinguished plenary talks that bridge the history and future of our field. The first talk will be delivered by Prof. Asad Abidi from UCLA, titled "RF-CMOS at 25: Some Unique Concepts That Endure."

Prof. Abidi will provide historical context on the motivations and challenges associated with developing RF and mm-Wave circuits on silicon. His presentation will specifically highlight RF CMOS architectures and circuits that were instrumental in achieving fine-grained calibration, significantly improving blocker tolerance, monolithically replacing oscillator modules, and enabling the migration of digital processing closer to the antenna.

Dr. Oliver Dial from IBM will deliver the second talk, titled "RF Control Systems for the Future of Quantum Computing." His presentation will focus on the pivotal moment in quantum computing as the field transitions toward fault-tolerant machines capable of executing millions of operations. This advancement is dramatically increasing the need for sophisticated control systems. Dr. Dial will explore the necessary evolution of dense, reliable, and low-power microwave signal generators and passives essential for controlling the tens of thousands of qubits anticipated in the near future.

Immediately following the Plenary, the RFIC Reception invites attendees to an engaging evening of social networking and technical exchange, supported by the RFIC 2026 Sponsors. Complimentary drinks and refreshments will be served as you explore highlights from the industry showcase and student paper finalists. This interactive setting allows for close-up discussions with authors demonstrating their work in a lab-like environment.

RFIC 2026 features two engaging panel sessions held during the lunch breaks. Monday kicks off with "Battle for RFIC Supremacy: Students versus Professionals," an event that blends education and entertainment in a lively game show format. On Tuesday, a joint panel with RFTT asks the critical question: "Will ML-AI Really Change Our Approach to Device Modelling and Circuit Design?" This session will dive into the 'topic of the hour'—AI—and debate its true impact on the future of our field.

Finally, RFIC 2026 concludes with a special farewell event: the Student-Industry ChipChat. This gathering provides a unique platform for the next generation of engineers, comprising students and young professionals, to connect with industry experts, discuss emerging technology trends, and gain valuable insights into their future careers. To celebrate the occasion, attendees will enjoy complimentary drinks and refreshments, with special gifts reserved for student participants.

Join the RFIC community in Boston, MA!.

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RFIC 2026 Schedule

Thomas M. Menino Convention & Exhibition Center

Saturday, 6 June 2026

08:00–17:00 Registration — North Lobby

Sunday, 7 June 2026

07:00–18:00 Registration — North Lobby
08:00–11:30 Workshops — 151AB, 152, 153AB, 153C, 154, 156AB, 156C, 157AB, 157C, 158, 252AB, 254AB, 255, 256, 257AB
11:30–11:45 Workshops Lunch Pickup — 258ABC
11:45–13:15 Technical Lecture — 253ABC: *Modern Receiver Architectures: Mixer-First, N-Path, and "No-Gain" Architecturess*
13:30–17:20 Workshops — 151AB, 152, 153AB, 153C, 154, 156AB, 156C, 157AB, 157C, 158, 252AB, 254AB, 255, 256, 257AB
17:30–19:00 RFIC Plenary — Ballroom
19:30–21:00 Welcoming Reception and Symposium Showcase — Westin Boston Seaport District Grand Ballroom

Monday, 8 June 2026

07:00–18:00 Registration — North Lobby
07:00–08:00 Speakers' Breakfast — 258ABC
08:00–11:50 Workshop — 157C
08:00–09:40 Mo1A — 252AB: *Industry Innovations in Transceivers and Beamformers for Communication and Radar*
08:00–09:40 Mo1B — 254AB: *Advanced LC-VCO Topologies for Ku- and Ka-Band*
08:00–09:40 Mo1C — 257AB: *Digital PAs and Transmitters*
08:00–09:40 Mo1D — 253ABC: *Components for Wireline Communications and Quantum Computings*
09:40–10:10 Coffee Break — Meeting Room Foyers
10:10–11:50 Mo2A — 252AB: *mm-Wave and Sub-THz Transmitters and Receivers*
10:10–11:50 Mo2B — 254AB: *High-Frequency LO Generators and VCOs*
10:10–11:50 Mo2C — 257AB: *LEO SATCOM and FR3 Transmitter Front-Ends and Power Amplifiers*
12:00–13:20 RFIC Panel Session — 253ABC: *Battle for RFIC Supremacy: Students versus Professionals*
13:30–15:10 Mo3A — 252AB: *Broadband Design Techniques for RF Amplifiers and Switches*
13:30–15:10 Mo3B — 254AB: *Advanced Frequency Conversion & Filtering Techniques*
13:30–15:10 Mo3C — 257AB: *Wideband and High-Efficiency PAs for D-Band and mm-Wave*
15:10–15:40 Coffee Break — Meeting Room Foyers
15:40–17:20 Mo4A — 252AB: *Integrated Radar and Spectrum-Sensing Arrays*
15:40–17:20 Mo4B — 254AB: *Front-Ends and LNAs*
15:40–17:20 Mo4C — 257AB: *Sub-THz Power Amplifiers and Bidirectional Amplifiers*
15:40–17:20 Mo4D — 253ABC: *Broadband and Bi-Directional Phase Shifters for RF and mm-Wave Arrays*

RFIC 2026 Schedule (continued)

Thomas M. Menino Convention & Exhibition Center

Tuesday, 9 June 2026

07:00–18:00 Registration — North Lobby
07:00–08:00 Speakers' Breakfast — 258ABC
08:00–09:40 Tu1A — 252AB: *mm-Wave FMCW Radars and UWB Transceivers*
08:00–09:40 Tu1B — 254AB: *Frequency Multipliers from D-Band to Sub-THz*
08:00–09:40 Tu1C — 257AB: *Scalable, Calibrated mm-Wave and Wideband Tx/Rx Front-Ends for Radar, 5G, and SATCOM*
08:00–09:40 Tu1J — 255: *High-Speed Optical Transceivers*
09:40–10:10 Coffee Break — Meeting Room Foyers
10:10–11:50 Tu2A — 252AB: *Broadband RF Front-End Components for Next-Generation Wireless Systems*
10:10–11:50 Tu2B — 254AB: *Advanced Phase-Locking and Clock Generation Techniques*
10:10–11:50 Tu2C — 257AB: *Next Generation Sub-THz Circuit Blocks*
10:10–11:50 Tu2J— 255: *Co-Packaged Optics and Die-to-Die Interfaces*
13:30–15:10 Tu3A — 252AB: *Recent Advances in GaN Technology*
13:30–15:10 Tu3B — 254AB: *Next-Generation CMOS Oscillators for RF and mm-Wave*
13:30–15:10 Tu3C — 257AB: *Advanced Integration Technologies for Power Amplifier and Low-Noise Amplifier Design*
15:10–15:40 Coffee Break — Meeting Room Foyers
15:40–17:20 Tu4A — 252AB: *Energy-Aware RF Techniques for Sensing and Communication*
15:40–17:20 Tu4B — 254AB: *mm-Wave Front-End Building Blocks for Signal Amplification and Generation*
15:40–17:20 Tu4C — 257AB: *Advances in Devices and Circuits for System Integration*
15:40–17:20 Tu4J — 255: *Transceiver Architectures for Ultra-Low Power IoT*
17:30–19:00 Student-Industry-Academia RFIChat — 259AB:
Catching the Next Wave: How to Spot the Next Big Thing and Make the Jump

RFIC Plenary, Reception, and Symposium Showcase

Sunday Evening, 7 June 2026

17:30–19:00
RFIC Plenary
Thomas M. Menino Convention & Exhibition Center (MCEC), Ballroom

Chair: Mohyee Mikhemar, Broadcom
Co-Chair: Bodhisatwa Sadhu, IBM

17:20 Doors opening and musical welcome
17:30 Welcome Message from Symposium Chair and TPC Chair
Student Paper Awards, Industry Paper Awards, Tina Quach Service Award
18:00 RF-CMOS at 25: Some Unique Concepts That Endure
Asad Abidi, University of California, Los Angeles
18:30 RF Control Systems for the Future of Quantum Computing
Oliver Dial, IBM

19:30–21:00
RFIC Welcoming Reception and Symposium Showcase
Westin Boston Seaport District (Westin), Grand Ballroom

The RFIC Interactive Reception highlights the Student Paper Awards finalists and the Industry Paper Awards finalists in an engaging social and technical evening event with food and drinks. Authors of these showcase papers will present their innovative work, summarized in poster format. This event is supported by the RFIC Symposium corporate sponsors.

Do not miss the RFIC Reception!

RFIC Plenary Speaker 1

Prof. Asad Abidi
Electrical and Computer Engineering,
University of California, Los Angeles

RF-CMOS at 25: Some Unique Concepts That Endure

Abstract: It would be wrong to view the dramatic rise of CMOS in mass-produced RF electronics as merely a way to lower costs or integrate more on a chip. CMOS introduced unprecedented circuits and architectures, enabling fine-grained calibration, substantial improvements in blocker tolerance, monolithic replacement of oscillator modules, and digital closer to the antenna. Today, complete RF-CMOS transceivers (except for a front-end module) are but a small piece of large mixed-signal systems-on-a-chip. The Internet is accessed at high speeds primarily through wireless connections. IoT devices are gradually proliferating in both built and remote environments. Wireless sensing is everywhere. This presentation will select a handful of concepts and describe, in accessible technical terms, what makes them endure.

About Prof. Asad Abidi

Prof. Asad Abidi received the B.Sc. degree in Electrical Engineering from Imperial College, London in 1976, and the Ph.D. from the University of California, Berkeley in 1982. He worked at Bell Laboratories, Murray Hill until 1985, and then joined the faculty of the University of California, Los Angeles where he is Distinguished Professor of Electrical Engineering. With his students he has developed many of the radio circuits and architectures that enable today's mobile devices.

Prof. Abidi has received the 2008 IEEE Donald O. Pederson Award in Solid-State Circuits and the 2012 and 2022 Best Paper Awards from the IEEE Journal of Solid-State Circuits. In 2015, he was named an Outstanding Alumnus of the Berkeley EECS Department. He was elected Fellow of IEEE in 1996, Member of the US National Academy of Engineering in 2007, and Fellow of TWAS, the world academy of sciences, in 2010.

RFIC Plenary Speaker 2

Dr. Oliver Dial
IBM

RF Control Systems for the Future of Quantum Computing

Abstract: Quantum computing is at an inflection point. Three years ago, we had the first instances of quantum computers performing calculations that could not be directly simulated. This year, we believe quantum advantage will be demonstrated: verifiable examples of quantum computers performing calculations faster or more accurately than is possible on classical computer. However, unlocking the full power of quantum computing will require large-scale fault tolerant quantum computers: computers able to run hundreds of millions of operations on thousands of qubits with no errors. Advances in the error correcting codes that, in principle, make this possible have greatly reduced the overhead of such a machine, to the extent we now believe it will be possible by 2029. However, even with these advances, these machines will have tens of thousands of qubits. Controlling them will require the rapid maturation of quantum control systems, demanding new, dense, reliable, and low power microwave signal generators, wiring, and passives to be designed, tested, and manufactured in the next few years. I will discuss how we foresee this evolving, and some of the requirements these RF control systems will have to achieve.

About Dr. Oliver Dial

Dr. Oliver Dial was named an IBM Fellow in 2021 for his contributions to quantum computing hardware. He is VP of Quantum Systems at IBM, ensuring IBM's quantum hardware and software together deliver an outstanding experience. Oliver received his PhD from MIT in 2007 for research in two-dimensional electron and hole systems. He then entered the field of quantum computing as a post-doc at Harvard, demonstrating the first two-qubit gate between semiconductor singlet-triplet qubits and performing pioneering charge noise spectroscopy in these systems. He joined IBM as a research scientist in 2012.

The Student Paper Awards Finalists

Chair: Jane Gu, Georgia Tech

The RFIC Student Paper Award aims to encourage student submissions and give finalists the opportunity to promote their research during the reception following the plenary session. This year's finalists, listed below, were nominated by the RFIC Technical Program Committee. A panel of judges from the committee selected the top three papers through a thorough review and discussion process. All finalists receive complimentary registration to the RFIC Symposium. The winners will be announced during the RFIC Plenary Session on 7 June 2026 and will each receive a plaque.

A 2.4-GHz Reconfigurable Digital Transmitter with Three-Vector-Synthesized IQ-Shared PA and Envelope Rotation Calibration for Multi-Standard IoT Applications
Linhao Ma, Zongle Ma, Qing Li, Hui Zhang, Dong Liang, Kai Li, Huan Yan, Keping Wang
Tianjin University, China
Mo1C-1 08:00

INFINITY: A 245–310GHz InP-FinFET CMOS Co-Packaged Sliding-IF Transmitter with On-Chip Resonant Cavity Antenna
Berke Gungor[1], Senne Gielen[2], Yang Zhang[2], Mark Ingels[2], Patrick Reynaert[1]
[1]KU Leuven, Belgium, [2]imec, Belgium
Mo2A-1 10:10

A D-Band Variable-Gain Balanced Power Amplifier with 36% FBW, 18.2dBm PSAT and Reconfigurable Adaptive Bias in 22-nm FD-SOI
Giacomo Venturini, Patrick Reynaert
KU Leuven, Belgium
Mo3C-1 13:30

A W-Band RTWO-Based Digital Transmitter for PMCW Radar Achieving 14.9% Efficiency
Shaoqi Yang[1], Zhongjun Zhang[1], Weichen Tao[1], Yuhao Yang[1], Juncheng Deng[1], Jing Liu[2], Fujiang Lin[1], Robert Bogdan Staszewski[3], Liheng Lou[1], Yizhe Hu[1]
[1]USTC, China, [2]Hefei SCMI, China, [3]University College Dublin, Ireland
Mo4A-5 17:00

A 4-Channel Self-Synchronizing Receiver Array Without LO Distribution with Angle-of-Arrival Estimation
Subhan Zakir, Waleed Ahmad, Alireza Kiyaei, Atif H. Shah, Saeed Zeinolabedinzadeh
Arizona State University, USA
Mo4B-1 15:40

A Calibration-Free 55-to-70dBc H1 Rejection, 13.8% Efficiency, 102-to-120GHz CMOS Frequency Tripler Using Phase-Alignment Technique for Harmonic Recombination
Sarah Koop-Brinkmann, Victor Lasserre, Vadim Issakov
Technische Universität Braunschweig, Germany
Tu1B-1 08:00

A 25.4fs Jitter Fractional-N Digital PLL with an LC-Based Power-Gated Oscillator and Series-Resonance DCO
Daniele Lodi Rizzini[1], Michele Rossoni[1], Filippo Osio[1], Stefano Gallucci[1], Riccardo Moleri[1], Andrea Mazzanti[2], Andrea L. Lacaita[1], Simone M. Dartizio[1], Salvatore Levantino[1]
[1]Politecnico di Milano, Italy, [2]Università di Pavia, Italy
Tu2B-3 10:50

A 1.49pJ/b 4-Channel 256-Gb/s MRM-Based Coherent Co-Packaged Optics with Linear Carrier Phase Recovery
Pengyu Zeng, Marziyeh Rezaei, Daniel Sturm, Asha Rashmi Nayak, Hongyong Li, Sajjad Moazeni
University of Washington, USA
Tu2J-1 10:10

A 47-to-100GHz Oscillator-Embedded Artificial Transmission Line Based LO Generator Achieving Averaged FoMt of -193.7dBc/Hz
Wei Sun, Benyamin Fallahi Motlagh, Boxun Yan, Aydin Babakhani
University of California, Los Angeles, USA
Tu4B-3 16:20

Student Paper Contest Eligibility: The student must have been a full-time student (9 hours/term graduate, 12 hours/term undergraduate) during the time the work was performed. The student must also be the lead author of the paper and must present the paper at the Symposium.

The Industry Paper Awards Finalists

Chair: Vadim Issakov, Technische Universität Braunschweig

The RFIC Industry Paper Awards highlights outstanding industry papers. The six finalists are listed below. These papers received nominations from the TPC sub-committees and godparents in a doubleblind review. From these six papers, a two-stage review process was conducted by a committee of TPC judges to identify the top 3 papers that have the highest impact on the field of RFIC. These 3 winners will be announced at the RFIC Plenary Session in Boston where each winner will receive a plaque in recognition for their outstanding contribution.

A SiGe TXSIP for E-Band Point-to-Point Systems from 71 to 86GHz with >32dBm Output Power
Christoph Steinbrecher[1], Fatih Kocer[1], Julio Canelo[1], Ekrem Oran[1], Ozgun Serttek[1], Kasim Ayyildiz[1], Santosh Kudtarkar[1], Arun Raj[1], Sacid Oruc[2], Mete Coskun[2]
[1]Analog Devices, USA, [2]Analog Devices, Türkiye
Mo1A-4 09:00

An Area-Efficient NBA-MMS UWB Receiver with Capacitance Boosting and PVT-Robust RSSI for IEEE 802.15.4ab
Sumin Kang, Junhyeong Kim, Sinyoung Kim, Wonjun Jung, Jonghoon Myeong, Duyong Seo, Hyun-Gi Seok, Hyun-Chul Park, Chan-Hong Park, Joonsuk Kim
Samsung, Korea
Tu1A-4 09:00

A 55-GHz Bandwidth PAM-4 InP DHBT Photoreceiver Based on PD-TIA Co-Design for >112-GBd Optical Transceivers
Antoine Chauvet[1], Romain Hersent[1], Fabrice Blache[1], Filipe Jorge[1], Marie Da-Rocha-Amaro[1], Karim Mekhazni[1], Harry Gariah[1], Nil Davy[1], Colin Mismer[1], Virginie Nodjiadjim[1], Michel Goix[1], Agnieszka Konczykowska[1], Bertrand Ardouin[1], Christophe Caillaud[1], Abed-Elhak Kasbari[2], Achour Ouslimani[2]
[1]III-V Lab, France, [2]ENSEA-LÉA, France
Tu1J-4 09:00

A 5–7GHz Channel and Bandwidth Selective Shunt N-Path LNA Based Receiver with +6dBm OOC IB1dB, <-71dBm LO Re-Radiation for WiFi 7 Multi-Link Operation
Ran Krichman[1], Ashoke Ravi[2], Natan Ershengoren[1], Rotem Banin[2], Sashank Krishnamurthy[2], Uri Grosglik[1], Oded Tal[1], Nave Sharvit[1], Oren E. Avraham[1], Sarit Zur[1], Ofir Degani[1]
[1]Intel, Israel, [2]Intel, USA
Tu2A-1 10:10

A 60GHz LNA and PA Achieving 5dB NF and 35.6% Peak PAE in a Gate-All-Around (GAA) CMOS Process with Backside Power Delivery
Steven Callender[1], Ibukun Momson[1], Awani Khodkumbhe[2], Ali Niknejad[2], Said Rami[1], Stefano Pellerano[1]
[1]Intel, USA, [2]University of California, Berkeley, USA
Tu3C-3 14:10

Accurate, High Coverage On-Chip Built-In Self-Test Adopting Precision-Enhanced Power Detection and Multipath Loopback for mmWave Radar IC Measurements
Doyoon Kim, Kyunghwan Kim, Geonho Park, Goeun Baek, Byeong-Taek Moon, Hyun-Chul Park, Chan-Hong Park
Samsung, Korea
Tu4C-1 15:40

Industry Paper Contest Eligibility: The first author must have an affiliation from industry. The first author must also be the lead author of the paper and must present the paper at the symposium.

RFIC Reception and Symposium Showcase
Featuring Best Student/Industry Paper Showcase

Systems & Applications Forum Chair: Jennifer Kitchen, Arizona State University
Student Chair: Jane Gu, Georgia Tech
Industry Chair: Vadim Issakov, Technische Universität Braunschweig

Join us immediately following the plenary session for the RFIC Reception and Symposium Showcase, supported by the RFIC Symposium's corporate sponsors. This event blends social and technical interactions, featuring food, drinks, and a showcase of RFIC innovation. The reception will spotlight the Student and Industry Paper Award finalists via large electronic posters. It offers attendees an engaging preview of cutting-edge research. This is a unique opportunity to network, to get a taste of innovative research, and have an early look at select papers scheduled for presentation over the following two days. The list of participating authors was current as of 15 May 2026.

Student Paper Awards Finalists' Showcase

A 2.4-GHz Reconfigurable Digital Transmitter with Three-Vector-Synthesized IQ-Shared PA and Envelope Rotation Calibration for Multi-Standard IoT Applications
Linhao Ma, Zongle Ma, Qing Li, Hui Zhang, Dong Liang, Kai Li, Huan Yan, Keping Wang
Tianjin University, China
Mo1C-1 08:00

INFINITY: A 245–310GHz InP-FinFET CMOS Co-Packaged Sliding-IF Transmitter with On-Chip Resonant Cavity Antenna
Berke Gungor[1], Senne Gielen[2], Yang Zhang[2], Mark Ingels[2], Patrick Reynaert[1]
[1]KU Leuven, Belgium, [2]imec, Belgium
Mo2A-1 10:10

A D-Band Variable-Gain Balanced Power Amplifier with 36% FBW, 18.2dBm PSAT and Reconfigurable Adaptive Bias in 22-nm FD-SOI
Giacomo Venturini, Patrick Reynaert
KU Leuven, Belgium
Mo3C-1 13:30

A W-Band RTWO-Based Digital Transmitter for PMCW Radar Achieving 14.9% Efficiency
Shaoqi Yang[1], Zhongjun Zhang[1], Weichen Tao[1], Yuhao Yang[1], Juncheng Deng[1], Jing Liu[2], Fujiang Lin[1], Robert Bogdan Staszewski[3], Liheng Lou[1], Yizhe Hu[1]
[1]USTC, China, [2]Hefei SCMI, China, [3]University College Dublin, Ireland
Mo4A-5 17:00

A 4-Channel Self-Synchronizing Receiver Array Without LO Distribution with Angle-of-Arrival Estimation
Subhan Zakir, Waleed Ahmad, Alireza Kiyaei, Atif H. Shah, Saeed Zeinolabedinzadeh
Arizona State University, USA
Mo4B-1 15:40

A Calibration-Free 55-to-70dBc H1 Rejection, 13.8% Efficiency, 102-to-120GHz CMOS Frequency Tripler Using Phase-Alignment Technique for Harmonic Recombination
Sarah Koop-Brinkmann, Victor Lasserre, Vadim Issakov
Technische Universität Braunschweig, Germany
Tu1B-1 08:00

A 25.4fs Jitter Fractional-N Digital PLL with an LC-Based Power-Gated Oscillator and Series-Resonance DCO
Daniele Lodi Rizzini[1], Michele Rossoni[1], Filippo Osio[1], Stefano Gallucci[1], Riccardo Moleri[1], Andrea Mazzanti[2], Andrea L. Lacaita[1], Simone M. Dartizio[1], Salvatore Levantino[1]
[1]Politecnico di Milano, Italy, [2]Università di Pavia, Italy
Tu2B-3 10:50

A 1.49pJ/b 4-Channel 256-Gb/s MRM-Based Coherent Co-Packaged Optics with Linear Carrier Phase Recovery
Pengyu Zeng, Marziyeh Rezaei, Daniel Sturm, Asha Rashmi Nayak, Hongyong Li, Sajjad Moazeni
University of Washington, USA
Tu2J-1 10:10

A 47-to-100GHz Oscillator-Embedded Artificial Transmission Line Based LO Generator Achieving Averaged FoMt of -193.7dBc/Hz
Wei Sun, Benyamin Fallahi Motlagh, Boxun Yan, Aydin Babakhani
University of California, Los Angeles, USA
Tu4B-3 16:20

Industry Paper Awards Finalists' Showcase

A SiGe TXSIP for E-Band Point-to-Point Systems from 71 to 86GHz with >32dBm Output Power
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[1]Analog Devices, USA, [2]Analog Devices, Türkiye
Mo1A-4 09:00

An Area-Efficient NBA-MMS UWB Receiver with Capacitance Boosting and PVT-Robust RSSI for IEEE 802.15.4ab
Sumin Kang, Junhyeong Kim, Sinyoung Kim, Wonjun Jung, Jonghoon Myeong, Duyong Seo, Hyun-Gi Seok, Hyun-Chul Park, Chan-Hong Park, Joonsuk Kim
Samsung, Korea
Tu1A-4 09:00

A 55-GHz Bandwidth PAM-4 InP DHBT Photoreceiver Based on PD-TIA Co-Design for >112-GBd Optical Transceivers
Antoine Chauvet[1], Romain Hersent[1], Fabrice Blache[1], Filipe Jorge[1], Marie Da-Rocha-Amaro[1], Karim Mekhazni[1], Harry Gariah[1], Nil Davy[1], Colin Mismer[1], Virginie Nodjiadjim[1], Michel Goix[1], Agnieszka Konczykowska[1], Bertrand Ardouin[1], Christophe Caillaud[1], Abed-Elhak Kasbari[2], Achour Ouslimani[2]
[1]III-V Lab, France, [2]ENSEA-LÉA, France
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Ran Krichman[1], Ashoke Ravi[2], Natan Ershengoren[1], Rotem Banin[2], Sashank Krishnamurthy[2], Uri Grosglik[1], Oded Tal[1], Nave Sharvit[1], Oren E. Avraham[1], Sarit Zur[1], Ofir Degani[1]
[1]Intel, Israel, [2]Intel, USA
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A 60GHz LNA and PA Achieving 5dB NF and 35.6% Peak PAE in a Gate-All-Around (GAA) CMOS Process with Backside Power Delivery
Steven Callender[1], Ibukun Momson[1], Awani Khodkumbhe[2], Ali Niknejad[2], Said Rami[1], Stefano Pellerano[1]
[1]Intel, USA, [2]University of California, Berkeley, USA
Tu3C-3 14:10

Accurate, High Coverage On-Chip Built-In Self-Test Adopting Precision-Enhanced Power Detection and Multipath Loopback for mmWave Radar IC Measurements
Doyoon Kim, Kyunghwan Kim, Geonho Park, Goeun Baek, Byeong-Taek Moon, Hyun-Chul Park, Chan-Hong Park
Samsung, Korea
Tu4C-1 15:40

RFIC Panel Session

Monday, 8 June 2026
12:00–13:20
Room 253ABC

Panel Sessions Chair: Yao-Hong Liu, imec

Battle for RFIC Supremacy: Students versus Professionals

Panel Organizers and Moderators:
Travis Forbes, *Sandia National Laboratories*
Emily Naviasky, *IBM*

Panelists: **Andreia Cathelin**, *STMicroelectronics*
Aly Ismail, *Apple*
Alexandre Siligaris, *CEA-Leti*
Yazan Saad-Aldine, *Technische Universität Braunschweig*
Keith Liang, *University of Maryland*
Pradyot Yadav, *MIT*

Abstract: A quiz show battle for RFIC knowledge supremacy is brewing between students and experienced professionals. Will it be the experience of the career RFIC veterans or the students who have been in the classroom more recently? Come join this fun and interactive panel to find out!

Student-Industry-Academia RFIChat

Tuesday, 9 June 2026
17:30–19:00
Room **259AB**

Student Chair: Jane Gu, Georgia Tech

Catching the Next Wave: How to Spot the Next Big Thing and Make the Jump

Moderators:

Emily Naviasky, *IBM*
Zeshan Ahmad, *Coherent*
Jane Gu, *Georgia Tech*

Panelists: **Alyosha C. Molnar**, *Cornell University*
Anthony Hopf, *STR*
Arvind Narayananm, *GlobalFoundries*
Jin Zhou, *MediaTek*
Matthew G. Anderson, *Oso Semiconductor*
Najme Ebrahimi, *Northeastern University*
Oren Eliezer, *Samsung*

Abstract: What could be the next big wave? How would you prepare to catch it now? Join us for a discussion sure to make a splash!.

RFIC Technical Lecture

Sunday, 7 June 2026
11:45–13:15
Room **253ABC**

Chair: Vito Giannini, OLIX Computing

Modern Receiver Architectures: Mixer-First, N-Path, and "No-Gain" Architectures

Speaker: **Bram Nauta**, *University of Twente*

Abstract: In a classical receiver, the first thing designers do is add amplification immediately after the chip's RF input. This is usually done with a low-noise amplifier (LNA) and is often followed by selectivity and a mixer. This way, the mixer may be noisy, and its design becomes easier. In the current overcrowded radio spectrum, however, adding the first amplifier may result in significant distortion products at the LNA output. These cannot be removed anymore. Therefore, mixer-first architectures have emerged as a candidate for the first circuit after the chip's RF input. These architectures do not use a low-noise amplifier but instead use a low-loss passive mixer. These passive mixers exhibit very good linearity and offer the option of narrow-band RF filtering at the mixer input. This makes the mixer-first receiver a good candidate for applications where interference is a challenge. The RF filtering is achieved by exploiting the mixer in a so-called N-path filter, which is a filtering technique from forgotten times. New ideas such as higher-order filtering and passive voltage gain via capacitor stacking will also be presented in this lecture. An outlook of fully passive receivers, even without active linear amplification, is also given as a possible future direction.

About Prof. Bram Nauta

Dr. Bram Nauta is a distinguished professor of integrated circuit design at the University of Twente. His expertise is in analog and radio frequency circuit design. He served as the Editor-in-Chief of the IEEE Journal of Solid-State Circuits, was the program chair of the International Solid-State Circuits Conference, and served as the President of the IEEE Solid-State Circuits Society. In 2014, he received the "Simon Stevin Meester" award (500,000 Euros), the largest national award in the Netherlands for achievements in engineering sciences. In 2019, he received an ERC (European Research Council) Advanced Grant (2.5 Million Euros, personal grant). In 2023, he received the NWO Stevin Prize (1.5 Million Euros), the largest national science prize in the Netherlands, for "exceptional success in knowledge exchange and impact for society". He is a fellow of the IEEE, a member of the Royal Netherlands Academy of Arts and Sciences (KNAW), and the Netherlands Academy of Engineering (NAE).

Monday 8 June 2026
08:00–09:40
Room 252AB
Session Mo1A: Industry Innovations in Transceivers and Beamformers for Communication and Radar
Chair: Susnata Mondal, Intel, USA
Co-Chair: Arun Paidimarri, IBM, USA

Mo1A-1 08:00
Ethernet to RF: Single Chip ORAN 4TX/4RX 5G Radio Unit Base Station Transceiver

Kevin Gard, Jianxun Fan, Dicle Ozis, Gord Allan, Kashif Sheikh, Justin Fortier, Tony Montalvo, Bing Zhao, David McLaurin, Benjamin Babjak, Ionel Gheorghe, Bruce Wilcox, Manish Manglani, Adam Bray; Analog Devices, USA

Abstract: This paper presents the first RF-to-Ethernet Open Radio Access Network (ORAN) split 7.2A radio unit (RU) base station system-on-a-chip (SOC). In 16nm FinFET CMOS, the 4-TX, 4-RX transceiver provides 660 MHz large-signal BW and 800 MHz DPD synthesis BW, across LO frequencies from 400 MHz to 7.1 GHz. It supports full-band multicarrier (MC) operation in all TDD/FDD 3GPP bands for NR FR1, LTE, and NB-IoT radios. The SoC includes 2×10Gb/s or 2×25Gb/s Ethernet interface, four receivers, four transmitters, and a digital pre-distortion (DPD) feedback receiver (FBRX). Four PLLs provide digital/data converter clocks, Ethernet clocks and two RF LO signals. Digital interpolation, decimation, AGC, TX Power control, and calibrations are managed by an ARM M4 dual core processor and internal controllers. An ARM A55 quad core processor running Linux provides radio unit (RU) control and digital front-end (DFE) configurability. Internal calibration timing is adaptable to support 3G/4G/5G subframe timing requirements. The SOC includes a chip-to-chip interface and software (SW) infrastructure for operating two chips seamlessly for 8-TX, 8-RX, 2-ORX support. Total ORAN SOC power dissipation for dual band FDD 4TX/4RX/FBRX 800 MHz synthesis BW is 24.1W.

Mo1A-2 08:20

A 57–67GHz +14dBm 4-Channel Transmitter With 7-Bit Phase Shifter and Built-In Self-Test for Doppler-Offset Doppler Division Multiplexing FMCW Radar

Jeff Shih-Chieh Chien, Samrat Dey, Ying Chen, Mingyuan Li, Ivan Siu-Chuang Lu, Tienyu Chang, Wanghua Wu, Joonhoi Hur; Samsung, USA

Abstract: This paper presents a 57–67 GHz 4-channel transmitter (TX) in 28-nm bulk CMOS process and FCBGA package for frequency-modulated continuous wave (FMCW) radar. Each TX channel achieves an output power of 14–15.3 dBm in the high-power mode (HPM) and 8.6–11.6 dBm in the low-power mode (LPM), while maintaining >12.3% HPM and >5.4% LPM TX efficiencies and 25 dB gain control range across band of interest. In addition, each TX channel features a phase shifter with 1.4 degrees phase resolution suitable for Doppler-Offset Doppler Division Multiplexing FMCW radar applications. For monitoring and calibration, a built-in self-test (BIST) path through an OOK modulator from TX to receiver (RX) channels is embedded on-chip.

Mo1A-3 08:40

A K-Band Fully-Connected 4-Channel Beamforming Transmitter IC for LEO SATCOM in 65nm CMOS

Jongho Yoo, Junhan Lim, Seong-Mo Moon, Hakmin Lee, Hongkie Lim, Dong-Pil Chang; ETRI, Korea

Abstract: This paper presents a 4-beam, 4-channel fully-connected beamforming transmitter IC implemented in 65nm CMOS for K/Ka-band low Earth orbit (LEO) satellite communication downlinks. To reduce beamformer complexity and power consumption, a wideband low-loss two-stage I/Q generator directly drives a variable-gain amplifier array, enabling Cartesian-coordinate-driven phase shifting without look-up table-based calibration. To enhance linear output power, an analog linearization technique is applied to a two-stacked power amplifier. The single-channel single-beam measurement results demonstrate a peak small-signal gain of 26 dB with a 3-dB gain bandwidth of 17–20 GHz, less than 1.3° RMS phase error, and less than 0.2 dB RMS amplitude error with 7-bit phase steps. The transmitter achieves 19.7 dBm OP_{1dB} and 20.2 dBm P_{sat} with peak drain efficiency/power-added efficiency (PAE) of 35.9%/23.0% at 19 GHz. Using a 64-QAM OFDM signal, the measured average output power reaches 13.6 dBm at -25 dB EVM with 8.5% transmitter PAE.

Mo1A-4 09:00

A SiGe TXSIP for E-Band Point-to-Point Systems from 71 to 86GHz with >32dBm Output Power

Christoph Steinbrecher[1], Fatih Kocer[1], Julio Canelo[1], Ekrem Oran[1], Ozgun Serttek[1], Kasim Ayyildiz[1], Santosh Kudtarkar[1], Arun Raj[1], Sacid Oruc[2], Mete Coskun[2]; [1]Analog Devices, USA, [2]Analog Devices, Türkiye

Abstract: This paper presents an all-Silicon system-in-package transmitter covering the entire E-Band spectrum from 71 to 86 GHz for point-to-point microwave links. It integrates an upconverter (UPC), variable gain amplifier (VGA) and two power amplifiers (PA) which are flip-chip mounted in a low-cost 19 × 20 mm^2 LGA package with a WR12 waveguide interface. The integrated PAs combine 64 individual amplifier channels and achieve a P_{SAT} greater than 32 dBm. The TXSIP meets 5G NR EVM limits up to output powers of 29, 28 and 26 dBm for 1 GSym/s 4-QAM, 16-QAM and 64-QAM signals, respectively.

Monday 8 June 2026
08:00–09:40
Room 254AB
Session Mo1B: Advanced LC-VCO Topologies for Ku- and Ka-Band

Chair: Teerachot Siriburanon, University College Dublin, Ireland
Co-Chair: Hanli Liu, Zhejiang University, China

Mo1B-1 08:00
A 12–16.3-GHz 197.7-dBc/Hz-FOMT Harmonic-Shaping VCO Using Enhanced Common-Mode Resonance Expansion Based on a Triple-Tank Coupled Resonator

Jin Zhang, Miao Yu, Kaixue Ma; Tianjin University, China

Abstract: This paper presents a wideband, low-phase-noise harmonic-shaping voltage-controlled oscillator (VCO) featuring a novel common-mode resonance expansion (CMRE) technique. To expand the bandwidth of conventional harmonic-shaping VCOs, a triple-tank coupled resonator (TTCR) is employed to synthesize a high-order common-mode (CM) resonance. Besides, by closely separating the poles of the TTCR, CM impedance fluctuations and deep notches are effectively mitigated across the wide frequency range. This technology significantly expands the CM high-impedance bandwidth, thereby eliminating manual tuning to align the second-harmonic resonance. Consequently, the VCO maintains a highly symmetric oscillation waveform and a near-zero DC component of the effective impulse sensitivity function ($\Gamma_{eff,dc}$), which intrinsically suppresses flicker noise up-conversion. Fabricated in a 28-nm CMOS process, the VCO occupies a core area of only 0.056 mm^2 and covers a tuning range of 12–16.3 GHz (30.4%). It achieves a remarkable $1/f^3$ phase noise corner frequency of 130 kHz at 12 GHz, maintaining below 500 kHz across the full bandwidth. The measured best phase noise is -113.3 dBc/Hz at 1-MHz offset, resulting in a peak Figure-of-Merit with tuning range (FoM_T) of 197.7 dBc/Hz.

Mo1B-2 08:20
A 15–18.3GHz Upper Ku-Band LC-VCO Achieving 201dBc/Hz FoMA in 65-nm CMOS

Alan Nelson, Adarsh Yadav, Narahari N. Moudghalya, Abhishek Srivastava; IIIT Hyderabad, India

Abstract: This paper presents a low phase-noise LC-VCO for upper Ku-band operation using a Gm,eff-boosted core with a triple-coupled stacked transformer and noise-circulation. Fabricated in 65-nm CMOS, it achieves a 15–18.3 GHz (19.8%) tuning range, -114.8 dBc/Hz phase noise at 1 MHz offset, and FoM/FoMT/FoMA of 189.1/195.0/201.0 dBc/Hz. The VCO occupies 0.064 mm^2, consumes less than 9 mW from 1 V, and is suited for compact upper-Ku/mmWave synthesizers.

Mo1B-3 08:40

Cross-Coupled CMOS Series-Resonance VCO with 3rd-Harmonic Output and -142dBc/Hz Phase Noise at 10MHz Offset from 29.7GHz

Kemal Vural[1], Andrea Bilato[2], Guglielmo De Filippi[2], Andrea Mazzanti[1]; [1]Università di Pavia, Italy, [2]Fondazione Chips-IT, Italy

Abstract: A cross-coupled CMOS series-resonance VCO with efficient third-harmonic extraction is presented. Operation of the tank at series resonance enables low phase noise, while the N-type negative resistance of the active core shapes the tank voltage to enhance odd-harmonic content. The third harmonic is extracted using a doubly tuned series-parallel transformer that also provides consistent suppression of the fundamental component. Implemented in a 65-nm CMOS process, the VCO tunes from 8.45 to 9.91 GHz and delivers up to 9.3 dBm at 29.7 GHz with a phase noise of -142 dBc/Hz at 10 MHz offset. With a peak FoM of 187 dBc/Hz, the measured performance compares favourably with the state of the art.

Mo1B-4 09:00

Fundamental 9.9-to-30GHz 207dBc/Hz FoM_T Quad-Core Quad-Mode VCO Utilizing One-Coil-For-All Topology in 40nm CMOS

Changqi Zhou[1], Hao He[2], Haobin He[1], Hanlin Yang[3], Yi Liu[3], Zuojun Wang[4], Bin Li[1], Xiang Yi[1], Zhijian Chen[1]; [1]SCUT, China, [2]NUS, Singapore, [3]HKUST, China, [4]CityUHK, China

Abstract: This paper introduces a 9.9–30.0 GHz quad-core quad-mode VCO featuring a symmetric 2D folded 8-shaped inductor with an embedded triple-peak common-mode resonator (TPCR). The design employs a purely inductive switching scheme to maximize the frequency tuning range (FTR) and utilizes the ultra-wideband TPCR to minimize common-mode (CM) return-path phase fluctuation over the entire FTR. Measurement results demonstrate a continuous and uniform FTR of 101% across four modes, with phase noise (PN) of -128.6 to -135.8 dBc/Hz at a 10 MHz offset. The design achieves a peak FoM_T of 206.9 dBc/Hz and a peak FoM_{TA} of 218.1 dBc/Hz.

Monday 8 June 2026
08:00–09:40
Room 257AB
Session Mo1C: Digital PAs and Transmitters
Chair: Zhiming Deng, MediaTek, USA
Co-Chair: Song Hu, Apple, USA

Mo1C-1 08:00
A 2.4-GHz Reconfigurable Digital Transmitter with Three-Vector-Synthesized IQ-Shared PA and Envelope Rotation Calibration for Multi-Standard IoT Applications

Linhao Ma, Zongle Ma, Qing Li, Hui Zhang, Dong Liang, Kai Li, Huan Yan, Keping Wang; Tianjin University, China

Abstract: A fully integrated multi-standard digital transmitter featuring linearity enhancement is demonstrated, incorporating a reconfigurable digital modulator to support OOK/BPSK/QPSK/16-QAM multi-modulations and an on-chip envelope rotation calibration circuit to optimize the linearity of 16-QAM modulation. This architecture also employs a three-vector-synthesized (TVS) IQ-shared Class-E power amplifier (PA) to avoid the 3 dB power loss of IQ transmitter and the mismatch between amplitude modulation (AM) and phase modulation (PM) paths of polar transmitter, achieving high efficiency and high linearity. Implemented in 40 nm CMOS, it achieves 35.7% peak system efficiency (SE) with 5.08 dBm peak output power at 2.4 GHz and occupies a core area of only 0.15 mm^2. At a data rate of 8 Mbps, the EVM of 16-QAM modulation is optimized from -19.9 dB to -24.2 dB through envelope rotation calibration with an average SE of 19.1%, an average output power of 2.58 dBm, and an energy efficiency of 1.18 nJ/bit.

Mo1C-2 08:20
A 28.5dBm 3.3V/1.1V All-Digital Wi-Fi 7 Polar Transmitter Employing Triple-Stacked Doherty Class-G SC-DPA in 14nm Fin-FET

Naor R. Shay[1], Elad Solomon[2], David Ben-Haim[2], Eran Socher[1], Ofir Degani[1]; [1]Tel Aviv University, Israel, [2]Intel, Israel

Abstract: This work presents a novel class G topology that enables reliable triple-transistor stacking dual-supply in Switched-Capacitor Digital Power Amplifier working from 3.3/1.1 V. A glitch-free logic for smooth supply mode switching was implemented. A 28.5dBm/31.6% dual-core Doherty combining DPA at 2.3–2.6GHz was integrated in an all-digital polar transmitter using 14-nm Fin-FET node. An error vector magnitude (EVM)/power efficiency of -38dB/19% is measured at 2.412GHz and 7.3-dB backoff (dBBO) from Pmax, thus meeting MCS13 4096-QAM OFDM Wi-Fi7 requirement.

Mo1C-3 08:40

+28.5dBm 5–7GHz FIR and Doherty Polar DTX Achieving -155dBc/Hz OOC Noise for WiFi MLO Applications

Eli Borokhovich, Eran Socher, Ofir Degani; Tel Aviv University, Israel

Abstract: This work introduces the first implementation of mixed-domain FIR filtering in a +28.5dBm, 5–7GHz polar digital transmitter with Doherty load modulation, achieving -155dBc/Hz Rx-noise levels at configurable offsets while meeting WiFi 4k-QAM EVM requirements across 40/80/160MHz bandwidths. Utilizing 14nm Fin-FET technology, the design proposes an integrated and efficient solution for future wireless communication coexistence scenarios, reducing OOC noise without external filters.

Mo1C-4 09:00

A 12 Bit, 1.3GHz to 4.7GHz Switched Current Source RF Power-DAC Achieving -47.2dB EVM for 4096-QAM

Manuel Wittlinger, Jakob Finkbeiner, Raphael Nägele, Markus Grözing, Manfred Berroth, Georg Rademacher; Universität Stuttgart, Germany

Abstract: Measurement results of an integrated radio frequency power-digital-to-analog converter (RF power-DAC) with high linearity and bandwidth are presented. The power cells operate as switched current sources to increase linearity at low and medium power. The operating mode shifts to current mode class-D at high power to optimize both linearity and efficiency. The RF power-DAC achieves 28.5 dBm peak output power with peak drain efficiency (DE) and system efficiency (SE) of 44.1% and 42.0% at 2.1 GHz. The 3 dB power bandwidth from 1.3GHz to 4.7GHz is 3.4GHz, which corresponds to 113% of relative bandwidth. For a 5MBd 4096-QAM signal at 2.2GHz, up to -47.2 dB EVM and -54.3 dBc ACLR can be reached with 18.9 dBm average output power and 11.0% SE. For the entire frequency range, the EVM is at least -41.6 dB, making the RF power-DAC perfectly suited for frequency-agile applications.

Monday 8 June 2026
08:00–09:40
Room 253ABC
Session Mo1D:
Components for Wireline Communications and Quantum Computing

Chair: Sushil Subramanian, Intel, USA

Co-Chair: Mohamed I. Ibrahim, Cornell University, USA

Mo1D-1 08:00

Low Cost Wideband Continuous-Time Linear Equalizers (CTLE) Based on SiGe BiCMOS Phase Change Material (PCM) Switches

Tian Liang, Mir H. Mahmud, Hasan Al-Rubaye, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This work introduces passive and active wideband continuous-time linear equalizers (CTLEs) operating up to 110 GHz. These designs are realized using Tower Semi phase-change material (PCM) technology in a SiGe BiCMOS process. The passive design achieves a 16.4 dB equalization level while consuming no static power. The active design provides a maximum DC gain of 16.5 dB and around 19 dB of low frequency de-emphasis. Modulated measurements confirm the operation of both designs at 120 GBd without transmitter pre-distortion and scope equalization. These designs leverage the high-performance characteristics of an advanced SiGe process with PCM switches and are targeted for 200 GBd wireline communication systems.

Mo1D-2 08:20

A 1.28pJ/b 32Gb/s Digital Isolator Using Coupled-Line Transformer for High-Speed Data Links

Jinyu Zhang, Rongxiang Wu, Yan Huo, Zheng Wang; UESTC, China

Abstract: This paper presents a high-speed, energy-efficient and compact digital isolator using a coupled-line transformer (CLT) for high-throughput galvanically isolated data links. The isolator employs a broadband CLT built in the package substrate as the isolation barrier, enabling an efficient pulse-polarity baseband data transmission scheme without carrier modulation. A transceiver incorporating a transmitter with edge rate control and a receiver with damping and equalization is designed to realize robust and efficient data transmission across the isolation barrier. Fabricated in a 28-nm CMOS technology, the prototype achieves error-free (BER$<10^{-12}$) isolated data transmission at a record data rate of 32 Gb/s with an energy efficiency of 1.28 pJ/b, while occupying a compact core area of 0.034 mm^2.

Mo1D-3 08:40

A pnp-npn Folded Cascode 240-GS/s 2-to-1 Analog Multiplexer in Complementary 130-nm SiGe BiCMOS

Maaz Khurram[1], Truman Jian[1], Peter Schvan[2], Sorin P. Voinigescu[1]; [1]University of Toronto, Canada, [2]Ciena, Canada

Abstract: A new pnp-npn folded-cascode return-to-zero Analog Multiplexer (AMUX) topology is proposed. It minimizes the supply voltage without compromising speed compared to npn-only topologies by taking advantage of a complementary SiGe BiCMOS process with fast pnp SiGe HBTs. Record 240-GS/s operation is measured by sampling sinusoidal inputs on both phases of a 120-GHz clock. The AMUX also multiplexes two PAM-4 or NRZ PRBS-13 inputs to generate 192-GBaud (384-Gb/s) PAM-4 and 210-GBaud NRZ outputs, the highest symbol rates reported to date for a silicon-based transmitter. The AMUX consumes 0.7 W from 1.8 and 3.3V supplies.

Mo1D-4 09:00

A Cryo-CMOS Electron/Nuclear Spin Controller with Combined GHz/MHz Drivers for Color-Center Qubits

Mohamed A. Elbadry, Niels Fakkel, Luc Enthoven, Fabio Sebastiano, Masoud Babaie; Technische Universiteit Delft, The Netherlands

Abstract: Color centers in diamond are a promising quantum-computing platform due to their long coherence times and operation at elevated cryogenic temperatures. This paper presents a 40-nm cryo-CMOS digital-intensive controller that employs a class-D amplifier with a 1-bit ΔΣ quantizer to generate precise, low-noise MHz pulses for nuclear-spin control, and a polar architecture to produce envelope-shaped GHz pulses for electron-spin control. The controller further features merged differential GHz/MHz output drivers, enabling seamless mode switching between electron- and nuclear-spin control. Implemented in 40-nm CMOS and measured at 4 K, the controller meets the requirements for 99.99% qubit control fidelity and delivers higher output current with improved efficiency at higher operating frequencies compared to prior art.

Monday 8 June 2026
10:10–11:50
Room 252AB
Session Mo2A: mm-Wave and Sub-THz Transmitters and Receivers
Chair: Najme Ebrahimi, Northeastern University, USA
Co-Chair: Muhammad Waleed Mansha, Nokia-Bell Labs, USA

Mo2A-1 10:10
INFINITY: A 245–310GHz InP-FinFET CMOS Co-Packaged Sliding-IF Transmitter with On-Chip Resonant Cavity Antenna

Berke Gungor[1], Senne Gielen[2], Yang Zhang[2], Mark Ingels[2], Patrick Reynaert[1]; [1]KU Leuven, Belgium, [2]imec, Belgium

Abstract: This work presents a 245–310 GHz heterogeneously integrated InP-FinFET CMOS sliding-IF transmitter (TX) with an on-chip antenna. The system consists of a 16-nm FinFET CMOS die that implements the baseband amplifiers, I/Q upconverter and a first LO multiplication step. The 250-nm InP DHBT die implements a second LO multiplication step, a second upconversion mixer, a power amplifier and an on-chip antenna. In continuous wave measurements, the TX shows an EIRP of more than 10 dBm from 245–300 GHz, with a peak of 14.6 dBm at 267 GHz. The performance of the TX is validated with over-the-air modulated measurements up to 57 cm distance and with data rates up to 40 Gbps. To the author's best knowledge, the TX achieves the highest single-element EIRP among all >200 GHz transmitters with antenna on-chip implementations.

Mo2A-2 10:30
A Novel 128GHz 8-PSK Receiver Using an On-Chip Multi-Probed Interferometer for Direct Phase-to-Bits Demodulation

Runzhou Chen, Hao-Yu Chien, Boxun Yan, Chao-Jen Tien, Mau-Chung Frank Chang; University of California, Los Angeles, USA

Abstract: This work introduces a novel D-band receiver that enables direct phase-to-bits demodulation using an on-chip interferometer to bypass the traditional mixers and high-speed ADCs. The proposed architecture forms a standing wave on a $\lambda/2$ digitally-probed artificial dielectric transmission line (DiPAD-TL) by interfering with the incoming RF signal with a constant-phase reference LO. A 64-element power detector array and subsequent mixed-signal blocks along the DiPAD-TL are used to sample and identify the standing wave's peak for mapping the RF phases dynamically to the baseband symbols. An amplitude tracking loop ensures balanced LO/RF power to minimize traveling waves and to ensure demodulation accuracy. The prototype receiver in 16nm FinFET performs direct 1.5 Gb/s 8-PSK demodulation at 128 GHz frequency with 134 mW DC power.

Mo2A-3 10:50

Antenna-Integrated, Chip-Embedded Glass Packaging of 200-GHz Transceiver Modules

Yuya Nemoto[1], Xingchen Li[2], Madhavan Swaminathan[2], Mark J.W. Rodwell[1]; [1]University of California, Santa Barbara, USA, [2]Georgia Tech, USA

Abstract: This work reports 200-GHz transceiver modules built from die-embedded glass packages. Previously reported 200-GHz InP HBT transceivers are integrated with 4×2-array antenna-in-package (AiP) solutions. System performance is optimized by chip/package co-design. A single-channel 204-GHz wireless radio link across 7 meters is demonstrated, achieving 44 Gbps (11-Gbaud 16-QAM) with 14.14% associated rms error-vector magnitude (EVM). This is the first reported packaging result demonstrating system integration of a full G-band transceiver module with integrated AiP.

Mo2A-4 11:10

A 240Gb/s 0.51pJ/b D-Band Direct-Conversion Receiver with Injection-Locking Based Quadrature Correction in 28nm CMOS

Xiaohan Shen, Xiaodi Feng, Siyu Men, Haoyu Zhu, Ningsheng Xu, Chen Jiang; Fudan University, China

Abstract: Exploiting the D-band spectrum is critical for next-generation wireless communication systems. This work presents a direct-conversion D-band receiver featuring a mixer-first topology that maximizes bandwidth and linearity for ultra-fast data rates. A novel injection-locking based quadrature correction scheme is proposed for precise IQ phase imbalance calibration. A high-order harmonic injection-locking LO multiplier chain is adopted to minimize DC power consumption. Measurement results show that the receiver exhibits a low noise figure around 13.3dB. Achieving 240Gb/s under 16QAM modulation with an energy efficiency of 0.51pJ/b, this work demonstrates the highest data rate and energy efficiency among all reported state-of-the-art D-band receivers.

Mo2A-5 11:30

A 138-GHz Dielectric Waveguide Link with 4.87pJ/bit Efficiency in 28-nm CMOS

Jiacheng Guo, Xinsheng Cheng, Yixia Wang, Yuchi Liu, Jizhao Li, Li Du, Yuan Du; Nanjing University, China

Abstract: This work presents a fully integrated 138-GHz Dielectric Waveguide (DWG) communication link in a 28-nm CMOS process, addressing the critical challenges of high cost and excessive power consumption in DWG interconnects. The proposed low-cost packaging scheme, combining wire bonding, SIW transition, and transverse aperture coupling, achieves a low coupling loss of 5.2 dB. The dynamic bias adjustment of the PA and LNA enables power consumption optimization for different link lengths. Measurement results demonstrate that the link delivers a state-of-the-art energy efficiency of 4.87 pJ/bit at 1.5 m with a data rate of 17 Gbps. Although the data rate declines at 3 m, it still reaches the theoretical maximum rate predicted by the dispersion factor model, validating the effectiveness of the system design.

Monday 8 June 2026
10:10–11:50
Room 254AB
Session Mo2B: High-Frequency LO Generators and VCOs
Chair: Alexandre Siligaris, CEA-Leti, France
Co-Chair: Salvatore Finocchiaro, Qorvo, USA

Mo2B-1 10:10
A 140-GHz 9-mW Self-Calibrating Quadrature Generator
Long Kong; Fudan University, China

Abstract: A quadrature generator based on RC-CR circuits maintains a 90° phase separation independent of input frequency, while its amplitude imbalance is sensed by a novel amplitude detector and automatically corrected by an analog feedback loop. Implemented in 28-nm CMOS technology, the prototype draws 9 mW of power, and achieves 0.56-dB amplitude error and a ±1.3° phase error after de-embedding the systematic offset.

Mo2B-2 10:30
An 85.5-to-94.5-GHz W-Band Fully-Symmetric Quadrature LO Generator with a Fast Quadrature Calibration Technique, Achieving Closely Matched 61-fs_{RMS} Jitter and 41-dB IRR
Sarang Lee, Seohee Jung, Seohyeon Kwak, Seungjae Lee, Hoojung Lee, Jaehyouk Choi; Seoul National University, Korea

Abstract: This work presents a W-band fully symmetric quadrature LO (QLO) generator that produces I/Q outputs with closely matched low phase noise (PN) and accurate quadrature phase alignment. To overcome the structural limitations of conventional W/D-band QLO generators, the proposed design employs a cascaded architecture consisting of a low-jitter digital PLL (DPLL) followed by fully symmetric subsampling PLLs (SSPLLs). This symmetric structure inherently equalizes the PN of the I/Q outputs, while a DTC-based three-step fast quadrature calibrator — employing cross-sampling (CS) and direct phase-shift (DPS) techniques — achieves precise quadrature phase calibration within 200 ns. Fabricated in 28-nm CMOS, the proposed QLO generator achieves an RMS jitter of 61 fs (1 k – 100 MHz) for both I and Q outputs and an image rejection ratio (IRR) of 41 dB.

Mo2B-3 10:50

A 69.2–85.6-GHz LO Generator Achieving 192.2-dBc/Hz FoM and 201.4-dBc/Hz FoM_A with Current-Reused Coupled Frequency Tripler and Implicit Ninth Harmonic Extraction in 65nm CMOS

Shuo Tian[1], Kaitian Yang[1], Yong Chen[2], Xiaolong Liu[1]; [1]SUSTech, China, [2]Tsinghua University, China

Abstract: This paper presents an E-band local oscillator (LO) generator with a current-reused coupled frequency tripler and 9th harmonic extraction. By stacking and coupling two class-F oscillators in a single current branch operating at f_0 and $3f_0$, respectively, the proposed coupled frequency tripler optimizes both phase noise and power consumption. Furthermore, by extracting the implicit $9f_0$ harmonic through the frequency tripler, a wideband, low-phase-noise E-band LO generator is realized. Fabricated in a 65-nm CMOS process, the proposed prototype achieves a frequency tuning range of 21.1% from 69.2 to 85.6 GHz, with phase noise ranging from -121.2 to -126 dBc/Hz at a 10-MHz offset. The power consumption varies from 10.1 to 11.4 mW, thus yielding a peak figure-of-merit (FoM) of 192.2 dBc/Hz and a FoM_T of 198.7 dBc/Hz at the 10-MHz offset. The proposed LO generator occupies a compact core area of 0.12 mm^2, corresponding to a peak FoM_A of 201.4 dBc/Hz.

Mo2B-4 11:10

A 40-GHz Series-Resonance VCO with Windmill-Coupled F-Type Inductive Network Achieving -132.36dBc/Hz PN at a 10-MHz Offset

Chen Yu, Changwenquan Song, Shiyuan Zheng, Liang Wu; CUHK-Shenzhen, China

Abstract: This paper presents a series-resonance voltage-controlled oscillator (SR-VCO) featuring a windmill-coupled F-type (WCF) inductive network. The proposed WCF inductive network breaks the low-frequency limitation of conventional SR-VCOs, thereby extending the intrinsic low phase noise (PN) advantage of series-resonance operation to the millimeter-wave (mmWave) regime. The windmill-shaped coupling provides robustness against intra-core stage mismatches and improves area efficiency, while an inherent inductive voltage division avoids reliability issue without the frequency penalty associated with capacitive division. Fabricated in a 40-nm CMOS process, the prototype measures a frequency tuning range (FTR) of 38.08–42.19 GHz (10.2%) and a PN of -132.36 to -129.74 dBc/Hz at a 10-MHz offset, while consuming 40 mW from a 1-V supply, resulting in a peak figure of merit (FoM) of 188.3 dBc/Hz.

Monday 8 June 2026
10:10–11:50
Room 257AB
Session Mo2C:
LEO SATCOM and FR3 Transmitter Front-Ends and Power Amplifiers
Chair: Andreia Cathelin, STMicroelectronics, France
Co-Chair: Tolga Dinc, Texas Instruments, USA

Mo2C-1 10:10
A High Performance Complementary SiGe HBT Power Amplifier with a Three Conductor Coupled Line Four-Way Wilkinson Combiner Balun for Emerging K-Band LEO SATCOM Transmit Front-End IC

Seungkyun Lee, Yoongoo Kang, Inchan Ju; Ajou University, Korea

Abstract: This work reports first a high performance (HP) complementary SiGe (CSiGe) HBT K-band power amplifier (PA) for emerging LEO SATCOM. A HP PNP SiGe HBT, with f_T/f_{max} of 210/240 GHz, is adopted to the PA output stage for its large voltage excursion while a high speed (HS) NPN SiGe HBT at f_T/f_{max} of 400/400 GHz is utilized for the PA driver stage. To further boost its output power (P_{OUT}), a compact three conductor coupled line (TCCL) four-way Wilkinson combiner balun (WCB) is proposed. Fabricated in 0.13 μm CSiGe BiCMOS, the proposed PA at K-band shows measured peak P_{OUT} and PAE of 26.0 dBm and 35.5% at 18.0 GHz, respectively, with the highest power density of 2010 mW/mm^2. The PA delivers linear P_{OUT} of 20.5/20.2 dBm at 250/400 MHz symbol rates 64 QAM modulation. This CSiGe PA result provides a blueprint for the future of low cost, HP LEO SATCOM transmit (TX) front-end IC.

Mo2C-2 10:30
A Ka-Band CMOS 4-Element Beamforming Transmitter for LEO SATCOM Using PA with Negative-Feedback-Based Interstage Matching Network and Asymmetric Wilkinson Power Divider

Wonseob Lee[1], Hyungju Kim[1], Hyeonwon Song[1], Mingyu Lee[1], Sunwoo Kong[2], Seunghyun Jang[2], Hui-Dong Lee[2], Bonghyuk Park[2], Seungchan Lee[1], Jinseok Park[3]; [1]Chonnam National University, Korea, [2]ETRI, Korea, [3]UNIST, Korea

Abstract: A Ka-Band 4-element beamforming integrated circuit (BFIC) for low Earth orbit (LEO) satellite communication (SATCOM) ground terminals is presented. By employing a proposed negative-feedback-based interstage matching network in the power amplifier (PA), the proposed BFIC achieves high output power and high gain while maintaining sufficient stability margin and efficiency. In addition, the proposed matching network improves S_{22} and offers robustness against VSWR variations. To address the bandwidth limitation in high-gain transmitter, wideband asymmetric Wilkinson power divider (WPD) is also proposed. The divider with asymmetric in/out impedance eliminates matching networks, reduces insertion loss, and extends bandwidth. The proposed BFIC is fabricated using 65-nm CMOS process with chip area of 2.07 mm × 3.58 mm. The BFIC delivers a saturated output power of 21 dBm and a gain of 41.8 dB with a TX total efficiency

of 28.9% and -18.5 dB of S_{22}. The 3-dB bandwidth is 3.6 GHz, ranging from 27.2 to 30.8 GHz It also achieves RMS gain and phase errors below 0.18 dB and 1.31°.

Mo2C-3 10:50

A Watt-Level, Thermally Reliable Ku-Band SiGe HBT Cascode Flip-Chip Power Amplifier Module Using an Optimal IC-to-Package ElectroThermal Codesign for LEO SATCOM Transmit Front-End

Seungpyo Han[1], Minchul Kim[2], Inchan Ju[1]; [1]Ajou University, Korea, [2]MMII Laboratory, Korea

Abstract: This work presents a compact, Watt-level SiGe HBT flip-chip power amplifier module (PAM) for emerging low earth orbit (LEO) SATCOM transmitter (TX) front-end. To attain high power yet thermal ruggedness, two differential SiGe HBT cascodes are combined through a four-way transformer balun, with so-called IC-to-Package ElectroThermal (ETH) codesign. Optimal layout of the PA output stage, copper pillar (CuP) bumps, and a laminate interposer are combined in ETH codesign, which decreases thermal resistance (R_{th}) of PAM by 14.8%, and it is verified through both thermal simulation and measurement. Fabricated in 0.13 μm SiGe BiCMOS, measured saturated output power (P_{SAT}) and peak PAE of the thermally optimized Ku-band SiGe PAM are 28.7 dBm and 36.8% at 10.7 GHz, respectively, and remain 28.2 dBm and 34.8% at T_{amb} = 85°C. The proposed ETH codesign enables the first success of delivering products to rapidly expanding Ku-band SATCOM user terminal market.

Mo2C-4 11:10

Top-Metal-Only RFIC Retargeting for Fast Specs-to-Silicon Iteration Enabled by AI-Assisted Inverse Design

Chenhao Chu[1], Yuqi Liu[1], Yizhou Xu[1], Shouqing Fu[2], Takuma Torii[3], Shintaro Shinjo[3], Konstantinos Manetakis[2], Andreas Burg[4], Hua Wang[1]; [1]ETH Zürich, Switzerland, [2]CSEM, Switzerland, [3]Mitsubishi Electric, Japan, [4]EPFL, Switzerland

Abstract: AI and machine learning (ML) are increasingly used to accelerate Radio-Frequency Integrated Circuit (RFIC) design, where specs-to-layout inverse-design automation can shorten design cycles and lower the expertise barrier. In practice, RFIC turnaround and design migration are constrained not only by iterative EM-driven passive design, but also by layout-to-silicon latency dominated by long fabrication cycles and the cost of full-mask preparation. To address these challenges, this paper presents a fast specs-to-silicon iteration framework for RFIC retargeting by reusing all lower-metal layers that define active devices and tuning elements (e.g., capacitors and resistors), while redesigning EM passives implemented in the reconfigurable top-metal stack above a reference mid-metal layer. We employ an AI-assisted template-seeded approach that enables fast inverse design of multi-metal-layer EM passives. As a proof of concept, two FR3 power amplifiers (PAs) at 13 and 20 GHz are designed in the GlobalFoundries 22nm FDX+ using top-metal-only routing and pixelated matching networks. PA1 measures an OP_{1dB} of 18.75–21.74 dBm, a PAE_{OP1dB} of 19.84%–32.65%, a P_{sat} of 19.89–22.13 dBm, and a PAE_{sat} of 19.89%–33.66% across 12.5–17 GHz. PA2 measures an OP_{1dB} of 16.00–17.68 dBm, a PAE_{OP1dB} of 18.70%–23.34%, a P_{sat} of 17.70–18.55 dBm, and a PAE_{sat} of 20.45%–24.10% across 19–24 GHz.

Monday 8 June 2026
13:30–15:10
Room 252AB
Session Mo3A:
Broadband Design Techniques for RF Amplifiers and Switches

Chair: Hsieh-Hung Hsieh, TSMC, Taiwan
Co-Chair: Shintaro Shinjo, Mitsubishi Electric, Japan

Mo3A-1 13:30

A 2-to-18GHz Reconfigurable LNA Using Direction Switchable Coupling Presenting 0.78-to-1.24dB NF in 0.15-μm GaAs pHEMT

Hao Ning, Zhaowu Wang, Yijie Zhang, Xinyan Li, Xiaochen Tang, Yong Wang; UESTC, China

Abstract: This paper presents a wideband low-noise amplifier (LNA) based on the proposed direction switchable coupling (DSC) architecture. The design features an input stage with a drain-source coupled line (DSCL) optimized for wideband noise and matching performance, rather than high-frequency gain boosting. The reconfigurable gain stage employs a DSC network integrated with a high-band compensation amplifier and an absorptive switch to split the band into low and high frequency paths, enabling precise gain compensation without introducing significant loss or complicating the matching network. Fabricated in 0.15-μm GaAs pHEMT technology, the prototype achieves a noise figure of 0.78-to-1.24 dB, a gain flatness of 1.8 dB, and an OP1dB of 9.67-to-11.11 dBm across 2-to-18 GHz bandwidth, demonstrating a competitive figure of merit compared to the state-of-the-art.

Mo3A-2 13:50

MIM Capacitor-Assisted Inverse Design of Nonintuitive Amplifiers

Vinay Chenna, Hossein Hashemi; University of Southern California, USA

Abstract: An algorithmic inverse-design technique is presented for the synthesis of nonintuitive amplifiers that enables the insertion of variable-sized metal-insulator-metal (MIM) capacitors directly into multilayered pixelated amplifier layouts. This capability expands the accessible design space and further improves the performance of pixelated radio frequency integrated circuits (RFICs). A hybrid real-binary optimization algorithm jointly co-optimizes the passive networks, transistor sizing and biasing, while autonomously determining the number, size and placement of MIM capacitors across multi-stage amplifier layouts. A SiGe HBT mm-Wave low-noise amplifier (LNA) synthesized using this approach experimentally achieves a gain-bandwidth product exceeding 1 THz with unconditional stability and a DC power consumption of 26 mW.

Mo3A-3 14:10

A Broadband Distributed Low-Noise Amplifier with Full-Band Noise Optimization and Built-In Balun

Yidong Fang[1], Lianbo Liu[1], Hao Guo[2], Taiyun Chi[2], Sensen Li[1]; [1]University of Texas at Austin, USA, [2]Rice University, USA

Abstract: This paper presents a distributed low-noise amplifier (LNA) achieving over 100 GHz bandwidth with full-band noise optimization. The proposed design inherently provides balun functionality, enabling direct interfacing with commonly employed single-ended antennas and balanced mixers. Dominant noise sources across different frequencies are identified and mitigated using targeted noise-canceling techniques and optimization strategies. At low frequencies, gate-termination noise is canceled using an active termination. At mid frequencies, a common-drain buffer followed by common-source and common-gate amplifiers enables channel-noise cancellation within the active core while preserving wide bandwidth and balun operation. At high frequencies, the noise transfer function is optimized to suppress gate-noise contributions by selecting an optimal number of distributed elements. The fabricated LNA occupies 0.24 mm^2 and demonstrates a measured 6–110 GHz bandwidth with over 10 dB gain, achieving a minimum noise figure of 2.21 dB and 0.034 dB/GHz flatness. The full-band noise performance is comparable to state-of-the-art single-frequency LNAs, and the LNA supports wideband modulation of 34/27 Gb/s 16-/64-QAM with low EVM.

Mo3A-4 14:30

A Broadband Distributed Amplifier Extending the Operation Frequency to $0.944f_T$

Jianquan Hu[1], Changzi Xie[2], Fanyi Meng[1], Kaixue Ma[1]; [1]Tianjin University, China, [2]CAEP, China

Abstract: This paper presents an ultra-broadband distributed amplifier (DA) with operation frequency from dc to $0.944f_T$. A novel gain cell of improved Darlington cascode with stacked transistor is proposed. The gain of proposed gain cell at high operation frequency is dramatically improved since the gain roll-off at high operation frequency caused by parasitic capacitances of transistors are suppressed by the nature of proposed topology. Along with several gain-peaking techniques, the gain bandwidth of DA using the proposed gain cell is significantly extended. The presented DA is fabricated by using 0.25-μm GaAs E/D-mode pHEMT process with 57-GHz transition frequency(f_T). Measurement results indicate that the implemented DA obtains a 11.5-dB average gain, better than 7.5-dB input/output return loss, and 14.8-dBm typical saturated output power from the dc to 53.8 GHz ($0.944f_T$). To the best of authors' knowledge, the implemented DA achieves largest ratio of bandwidth to f_T among the DAs using similar process.

Mo3A-5 14:50

A DC-to-170GHz Broadband Distributed SPDT-Switch and Power-Combiner Combo with Source Switch Control

Yidong Fang[1], Lianbo Liu[1], Song Hang Chai[1], Hang Wang[2], Taiyun Chi[2], Sensen Li[1]; [1]University of Texas at Austin, USA, [2]Rice University, USA

Abstract: This paper presents a CMOS-based DC–170 GHz wideband single-pole double-throw (SPDT) switch and power-combiner module, realized through a distributed topology and a source-controlled switching scheme. Unlike conventional gate-controlled designs, the proposed source-selection approach separates the RF and DC control paths and enhances isolation by enabling an effective negative transistor VGS without the need for negative voltage generation. The distributed two-way combining architecture not only ensures broadband impedance and delay matching, but also enables state-independent operation, allowing seamless reconfiguration between switching and variable gain combining modes within the same network. Fabricated in 22-nm FDSOI CMOS technology, the prototype occupies a compact 0.09 mm^2 core area and shows close agreement between simulation and measurement. The switch/combiner combo achieves 0–3 dB insertion loss and >15 dB return loss across the entire DC–170 GHz range, demonstrating instantaneous broadband operation without band-tuning or switching elements.

Monday 8 June 2026
13:30–15:10
Room 254AB
Session Mo3B: Advanced Frequency Conversion & Filtering Techniques
Chair: Tong Zhang, Google, USA
Co-Chair: Jesse Moody, University of Maryland, USA

Mo3B-1 13:30
A W-Band Low-Noise Switched-Gm Down-Conversion Mixer with Gm-Boosting Feedback and Trifilar Transformer in 65-nm CMOS

Benqing Guo[1], Jing Gong[2], Jun Chen[3]; [1]CUIT, China, [2]Sichuan University, China, [3]Huawei Technologies, China

Abstract: This paper presents a W-band low-noise down-conversion mixer implemented in 65-nm CMOS technology. The proposed mixer employs a switched-transconductance (SwGm) architecture with DC-decoupled RF and LO stages, overcoming the frequency limitations of conventional SwGm topologies. Transformers provide magnetic coupling between stages, enabling gm boosting and wideband impedance matching of RF and LO ports. The transformer feedback of RF Gm stage enhances conversion gain while simultaneously reducing noise figure through partial noise cancellation. A pseudo-differential RF stage is adopted to improve linearity under limited voltage headroom. The LO stage noise is inherently cancelled in common mode, and sinusoidal switching minimises noise folding from the RF Gm stage. The mixer achieves 12.2 dB conversion gain, 5.0 dB noise figure, and 0.8 dBm IIP3 at 88 GHz, while consuming 6 mW from a 0.6-V supply. The measured results demonstrate excellent performance for W-band receiver applications.

Mo3B-2 13:50
A Broadband Fully-Distributed Mixer-First Receiver Achieving 40–128GHz RF Bandwidth

Zhaojing Fu[1], Hao Yu[1], Gerald Topalli[2], Taiyun Chi[2], Sensen Li[1]; [1]University of Texas at Austin, USA, [2]Rice University, USA

Abstract: This work presents a broadband mixer-first receiver implemented in a fully distributed topology that employs polyphase harmonic-cancellation to realize octuple local oscillation (LO) signal generation with multi-octave bandwidth. A wideband, three-stage, transformer-based passive quadrature signal-generation network and a distributed active balun are implemented to provide accurate polyphase signals over a broad frequency range. Fully distributed push-push quadrupler and doubler stages achieve frequency octupling across a 32–156 GHz bandwidth. A polyphase harmonic-cancellation technique is employed to suppress undesired spurious tones without compromising bandwidth. Moreover, a distributed active mixer is co-designed with the distributed LO generator to ensure broad RF coverage. The resulting fully distributed mixer-first receiver covers 40–128 GHz RF bandwidth, achieving a peak conversion gain of -7.6 dB with a total DC power consumption of 122 mW, enabling access to a wide spectrum.

Mo3B-3 14:10

An FR3 Simultaneous Dual-Carrier Passive Mixer-First Diplexer Receiver Front-End Achieving 6.4dB NF and -3.2dBm B1dB

Jamie C. Ye, Alain H. Antón, Alyosha C. Molnar; Cornell University, USA

Abstract: A low-power high-dynamic-range passive mixer-first diplexer receiver front-end is presented for the 6G FR3 band. The architecture simultaneously down-converts two arbitrary bands through a single RF port and consists of two passive mixers in parallel, each coupled to the antenna by $\lambda/4$ impedance transformers that minimize cross-loading while providing impedance transparency and out-of-band (OOB) filtering. The architecture achieves high performance with low power consumption by driving the mixers directly with integrated Class F-1 harmonically enhanced (HE) quadrature oscillators. The 11.8–13.9 GHz prototype is implemented in a 16nm FinFET process and achieves a 6.4 dB noise figure (NF), -3.2dBm OOB blocker compression (B1dB), and 10dBm OOB input-referred third order intercept point (IIP3) while consuming 12.7mW per channel.

Mo3B-4 14:30

A 6GHz 3× Subharmonic Mixer with 12.4-dB Conversion Gain and 73-dB Fundamental Rejection

Ahmed R. Aboulsaad, Zhuoran Wu, Noah Levy, Jacques C. Rudell; University of Washington, USA

Abstract: This paper presents a 6-GHz 3× subharmonic down-conversion mixer achieving 12.4-dB peak conversion gain and 73-dB fundamental rejection, the highest reported performance among down-conversion 3× subharmonic mixers. The proposed architecture employs a two-stage fundamental-cancelation scheme consisting of a tunable L-C coarse band-stop network followed by an active feed-forward fine canceler, enabling phase-invariant suppression without requiring multi-phase LO generation or precise phase matching. Fabricated in 180-nm CMOS, the prototype consumes 41mW including LO buffers and output drivers. Measurement results demonstrate wideband operation, low sensitivity to LO drive level, and state-of-the-art suppression of undesired fundamental mixing products, making the design suitable for next-generation WLAN receivers operating in the 6-GHz band.

Mo3B-5 14:50

A 1.5–4-GHz Reconfigurable N-Path Notch Filter with >40-dBc Rejection and >15-dBm B1dB

Gucheng Zhou[1], Ziyuan Chen[1], Xiong Chen[1], Pei-Ling Chi[2], Tao Yang[1]; [1]UESTC, China, [2]NYCU, Taiwan

Abstract: A reconfigurable N-path notch filter with enhanced notch rejection and power-handling capability is presented. The proposed architecture employs a hybrid reflective-absorptive mechanism that decouples blocking power handling from switch linearity constraints. The filter comprises a 90° quadrature coupler, an N-path resonant unit, and a tunable passive resistor, where the resonant unit and resistor are connected in parallel and terminated at the through and coupled ports of the coupler. Under high-power excitation, desired signals are primarily reflected by the N-path resonator, while strong interferers are absorbed by the passive resistor, thereby significantly improving blocking rejection. A prototype implemented in a 65-nm CMOS process demonstrates a tunable notch frequency from 1.5 to 4 GHz, notch depth exceeding 40 dBc (up to 50 dBc) with a 120-MHz 3dB bandwidth, a measured B1dB above 15 dBm, and an IIP3 of 27 dBm, while occupying 0.9 mm^2 and consuming 14–33 mW.

Monday 8 June 2026
13:30–15:10
Room 257AB
Session Mo3C:
Wideband and High-Efficiency PAs for D-Band and mm-Wave

Chair: Hyun-Chul Park, Samsung, Korea
Co-Chair: Patrick Reynaert, KU Leuven, Belgium

Mo3C-1 13:30

A D-Band Variable-Gain Balanced Power Amplifier with 36% FBW, 18.2dBm P_{SAT} and Reconfigurable Adaptive Bias in 22-nm FD-SOI

Giacomo Venturini, Patrick Reynaert; KU Leuven, Belgium

Abstract: This paper presents a wideband variable-gain balanced power amplifier (VGPA) for D-band applications in 22nm FD-SOI. Guanella transformers are employed in both the power combiner and the stacked amplifier stages for low-loss and broadband matching, with their center tap utilized for supply feed and current steering. An adaptive bias network boosts the output referred compression point (OP_{1dB}) and enables reconfiguration of the VGPA to maximize either signal bandwidth or linearity. The proposed VGPA achieves a small-signal peak gain of 22.5 dB with a 3-dB fractional bandwidth (FBW) of 36% centered at 128.5 GHz, and a tuning range of 15 dB. The maximum measured saturated output power (P_{SAT}), OP_{1dB}, and peak power-added efficiency (PAE) are 18.2 dBm, 16.6 dBm, and 10%, respectively. The maximum measured data-rates are 20 Gb/s with 16-QAM in the high-BW configuration and 12 Gb/s with 64-QAM in the high-linearity configuration.

Mo3C-2 13:50

A 0.036mm^2, 145GHz CMOS Power Amplifier with 7.4% PAE_{1dB} and 4.2dBm OP_{1dB} for Large Arrays

Kwangwon Park, Mark J.W. Rodwell; University of California, Santa Barbara, USA

Abstract: We present 145 GHz power amplifiers (PAs) in 22-nm FD-SOI technology with state-of-the-art low DC power consumption and small die area. Two distinct linearization architectures are demonstrated: a PA using an adaptive back-gate voltage biasing network (ABN-PA), and a PA using diode-based linearization (DBL-PA). Both PAs use a balun output combiner. The ABN-PA achieves 12% peak power-added efficiency (PAE), 7.4% PAE_{1dB}, 7.8 dBm P_{sat}, and 24 dB small-signal gain using a 0.8 V supply. The core area, including supply bypass capacitors and ground wall surrounding transformers and baluns, is only 0.036 mm^2. To facilitate integration into dense large-scale arrays, the PA does not require areas of exclusion to metal density rules. To our knowledge, the PAs achieve the smallest die area, DC power consumption and highest PAE_{1dB} among reported D-band CMOS PAs.

Mo3C-3 14:10

A 9.5-to-40GHz Ultra-Broadband Linear Power Amplifier with Compensated Coupled-Line Transformer in 65-nm Bulk CMOS

Sangjin Yoo, Kyutaek Oh, Geuntae Kim, Ilku Nam, Ockgoo Lee; Pusan National University, Korea

Abstract: This paper presents a 9.5–40 GHz high-power, ultra-broadband linear power amplifier (PA) in 65-nm bulk CMOS technology for 5G FR2 and future 6G applications. To achieve such broadband high-power performance, a compensated coupled-line transformer (CCLT) is proposed. Based on even- and odd-mode analysis, the proposed CCLT absorbs the output capacitances of the device into the network while offering an arbitrary impedance transformation ratio. The prototype PA achieves a peak small-signal gain of 17.3 dB with a 3-dB bandwidth of 9.5–40 GHz. In continuous-wave measurements, the PA demonstrates a saturated output power of 21.8–23.8 dBm across 9–40 GHz, which corresponds to a 2-dB fractional bandwidth of 126.5%. Additionally, the PA achieves a maximum power-added efficiency (PAE) of 23.9%–40.4% across the band. Furthermore, under a 400-MHz 64-QAM 5G NR FR2 signal (9.7-dB PAPR), it delivers an average output power of 12.9–16.4 dBm and an average PAE of 5.2%–11.7% across 10–40 GHz.

Mo3C-4 14:30

A 15.5–46.0GHz Broadband Power Amplifier with 19.0–22.0dBm P_{sat} and 30.0% Peak PAE_{max} in 28-nm Bulk CMOS

Ting Huang, Hongtao Xu, Yun Yin; Fudan University, China

Abstract: This paper proposed a broadband power amplifier (PA) in 28-nm CMOS technology with a high-efficiency matching network. The output matching network achieves a passive efficiency greater than 65.0% over 17.2–50.8 GHz. Based on the matching network, the proposed PA demonstrates saturation power (P_{sat}) of 19.0 to 22.0 dBm over 15.5–46.0 GHz with a peak PAE_{max} of 30.0%. Under 600-MHz 256-QAM signal, the PA achieves P_{avg} of 13.3 dBm and PAE_{avg} of 6.1% with EVM/ACLR of -32.5 dB/-30.9 dBc at 25 GHz, which indicates that the PA is a good candidate for high-speed wireless communication systems.

Mo3C-5 14:50

A 37–43GHz VSWR-Resilient Load-Isolated Doherty Power Amplifier Achieving 26% Average PAE at 36Gb/s in 45-nm SOI CMOS

Yahia Ibrahim, Ali Niknejad; University of California, Berkeley, USA

Abstract: This paper presents a compact 40-GHz load-isolated Doherty power amplifier (PA) architecture with enhanced resilience to antenna voltage standing wave ratio (VSWR) variations. Doherty VSWR Resiliency is achieved by isolating the Doherty load-modulation network from the antenna through placing the network before the cascode transistor. The proposed PA achieves a peak output power (P_{sat}) of 20 dBm, an output 1-dB compression point (OP_{1dB}) of 19 dBm, and a power gain of 17.5 dB at 40GHz, with a small-signal gain bandwidth from 35.5 to 44.5 GHz. Peak power-added efficiency (PAE) exceeds 39%, while 25.5% PAE is achieved at 6-dB power back-off (PBO) from P_{sat}, with performance maintained over the 37–43 GHz frequency range. Under 64-QAM modulated signal operation, the PA achieves an average output power (P_{avg}) of 16 dBm at 0.6 Gb/s with 30% average PAE, and 15.5 dBm at 36 Gb/s with 26% average PAE. The proposed architecture demonstrates VSWR-resilient operation, maintaining an average PAE above 24.5% under worst-case 2:1 VSWR phase conditions. The PA occupies a compact core area of 0.225 mm^2.

Monday 8 June 2026
15:40–17:20
Room 252AB
Session Mo4A: Integrated Radar and Spectrum-Sensing Arrays
Chair: Harald Pretl, Johannes Kepler Universität Linz, Austria
Co-Chair: Mustafijur Rahman, IIT Delhi, India

Mo4A-1 15:40
A 4T4R Code-Domain UWB Radar with Fully Analog Multi-Lag Correlators and Pre-Correlation Averaging

A. Undavalli[1], A.S. Kumar[2], T.G. Liang[1], K. Rashed[3], S. Chakrabartty[4], A. Natarajan[2], A. Nagulu[1];
[1]Northeastern University, USA, [2]Yale University, USA, [3]Oregon State University, USA, [4]WashU, USA

Abstract: This work presents a fully-integrated, 16-VRX quasi-monostatic radar with four transmitters, four receivers, and analog I/Q correlators in a 22nm SOI CMOS for indoor sensing and simultaneous multi-user operation. The radar operates from 4.5 to 9 GHz with a 1 GHz modulation frequency. The high-speed ADC and memory requirements were reduced by 50× using the proposed pre-correlation averaging and an analog multi-lag I/Q correlator. The prototype delivers 9.1dBm peak power at 6 GHz, achieving a >3.5m range, range resolution of 5.6 cm, RMS range error of 1.8 cm, ±30° field of view in azimuth and elevation, and RMS angular error of 1.5°. The 16-VRX radar consumes 1.5 μJ/frame (i.e., 94 nJ/channel/frame), representing a state-of-the-art energy efficiency for a UWB MIMO radar system.

Mo4A-2 16:00
A 2 to 20GHz Resolution-Enhanced RF Spectrum Sensor Using a Looped Phase-Time Array

Liwen Zhong, Meijun Tian, Wooram Lee; Penn State, USA

Abstract: This paper presents a 2-to-20 GHz RF signal processor based on a looped phase-time array that significantly enhances frequency resolution for ultra-broadband spectrum sensing. In prior phased-array-inspired RF signal processors, the achievable resolution bandwidth scales inversely with the number of array elements, leading to fundamental trade-offs among frequency resolution, chip area, and power consumption. By looping the phase-time array, the proposed architecture emulates the response of an infinite-element array, effectively overcoming these trade-offs. The signal processor is fabricated in a 22-nm FD-SOI process and achieves an average resolution bandwidth of 1.6 GHz (3.3 GHz for loop off), a frequency step of 0.8 GHz, and a scanning range from 2 to 20 GHz, while consuming 122 mW of power and occupying a core area of 3.9 mm^2.

Mo4A-3 16:20

405-GHz 2×2 Concurrent Transceiver Pixel Array with 7.8-GHz Bandwidth Using Series-Coupled Standing-Wave Oscillators

Seungmo Noh[1], Goutham Murugesan[1], Seongjae Mun[1], Young-Joon Lee[1], Frank Zhang[1], Wooyeol Choi[2], Kenneth K. O[1]; [1]University of Texas at Dallas, USA, [2]Seoul National University, Korea

Abstract: A 405-GHz 2×2 array of concurrent transceiver pixels integrating a 202.5-GHz frequency tripler, a push-push VCO and a subharmonic mixer, an IF LNA, and a patch antenna in an area smaller than $(\lambda/2)^2$ is used to demonstrate the techniques for scaling up concurrent transceiver pixel arrays while increasing the frequency injection locking range. The array fabricated in 22-nm FDSOI CMOS employs an injection-locked H-shaped standing-wave oscillator with a series-type current mode coupling for pixel synchronization that enables wideband locking, a 90° feed to the pixel array without mutual interference and antenna-orientation misalignment. The array exhibits a locking range of 7.8 GHz, a peak EIRP of -3.3 dBm, and a minimum pixel DSB noise figure (NF) of 30 dB at 221.2-mW DC power consumption. The pixel NF is the lowest and the locking range is the widest (8.7×) among that for concurrent transceiver pixel arrays. It is also the first demonstration of a 2-D pixel array realized as a 2×2 prototype.

Mo4A-4 16:40

A Doppler-Assisted 76GHz PMCW Radar with Meter-Scale Unambiguous Range and μm-Scale Range Accuracy

Zhengyang Zhang, Xuyang Liu, Yilun Huang, Hamidreza Aghasi; University of California, Irvine, USA

Abstract: This work presents a radar transceiver (TRX) featuring a hybrid operation scheme, where Doppler-CW and PMCW are employed in distinct frequency bands to enable cooperative sensing. By synchronizing the PRBS generator of PMCW radar and the Doppler radar carrier signal, the joint operation achieves range accuracy down to tens of μm without range ambiguity. The radar chip is fabricated in 65 nm CMOS technology, occupies 1.55 mm^2 of area and consumes 329.7 mW of power, demonstrating 0.18° of phase accuracy leading to 50 μm range accuracy with a meter-scale unambiguous range.

Mo4A-5 17:00

A W-Band RTWO-Based Digital Transmitter for PMCW Radar Achieving 14.9% Efficiency

Shaoqi Yang[1], Zhongjun Zhang[1], Weichen Tao[1], Yuhao Yang[1], Juncheng Deng[1], Jing Liu[2], Fujiang Lin[1], Robert Bogdan Staszewski[3], Liheng Lou[1], Yizhe Hu[1]; [1]USTC, China, [2]Hefei SCMI, China, [3]University College Dublin, Ireland

Abstract: This work presents a compact and highly efficient W-band digital transmitter for phase-modulated continuous-wave (PMCW) radar applications. A rotary traveling-wave oscillator (RTWO) with an embedded edge-combining upconverter simultaneously performs frequency quadrupling and BPSK modulation, eliminating the need for mm-wave LO buffers. Phase shifting (PS) is realized in the charge domain using a capacitive DAC within a charge-steering sampling (CSS) all-digital phase-locked loop (ADPLL), enabling a low-overhead and power-efficient path for phased-array operation. Fabricated in 22-nm CMOS, the transmitter occupies 0.144 mm^2 and delivers 18dBm peak output power with a maximum efficiency of 14.9%. PS is measured in both single- and dual-channel configurations, demonstrating a 409.7 fs (2.8°) step size and an RMS phase error of 55.6 fs (0.38°). In summary, the proposed architecture offers state-of-the-art TX efficiency and integration density for W-band radar transmitters, while providing intrinsic phase-shifting capability at the channel level for scalable PMCW radar arrays.

Monday 8 June 2026
15:40–17:20
Room 254AB
Session Mo4B: Front-Ends and LNAs
Chair: Vojkan Vidojkovic, TU/e, The Netherlands
Co-Chair: Marcus Granger-Jones, Qorvo, USA

Mo4B-1 15:40
A 4-Channel Self-Synchronizing Receiver Array Without LO Distribution with Angle-of-Arrival Estimation

Subhan Zakir, Waleed Ahmad, Alireza Kiyaei, Atif H. Shah, Saeed Zeinolabedinzadeh; Arizona State University, USA

Abstract: We present a 4-channel self-synchronizing binary-phase-shift keying (BPSK) receiver array in which each channel autonomously locks to the incoming carrier, enabling direct-conversion operation without the need for a local oscillator (LO) distribution network or synchronization. Each channel generates its own demodulated data stream, enabling either coherent combining for enhanced signal-to-noise ratio or independent processing to realize spatial diversity. Since the architecture eliminates LO distribution and each branch performs its own carrier recovery and demodulation, the system is inherently scalable. With each receiver branch employing an independent phase-locked loop (PLL) that locks to the received carrier, the system preserves the inter-element phase relationships imposed by the arriving wavefront. Consequently, the relative phase across channels can be exploited for angle-of-arrival estimation and angular localization. Each channel employs a two-stage low-noise amplifier (LNA) followed by a 28 GHz PLL. The 4×1 receiver chip is implemented in 130 nm SiGe BiCMOS technology.

Mo4B-2 16:00
A 24–29.5-GHz CMOS Front-End Module with 33.6% TX Peak Efficiency and 5.8-mW RX Power Consumption

Dong-Jun Shin, Songcheol Hong; KAIST, Korea

Abstract: This paper presents a 24–29.5-GHz front-end module (FEM) integrating a differential high-efficiency power amplifier (PA), a single-ended low-power low-noise amplifier (LNA), and a matching-network-embedded (MNE) antenna switch that supports fifth-generation (5G) frequency range 2 (FR2) bands (n257, n258, and n261). The highly linear class-AB PA is designed to mitigate AM-PM distortion without degrading output power. A single-ended half-supply-voltage configuration is adopted to reduce LNA power consumption without sacrificing linearity. In addition, an MNE antenna switch configuration for the differential PA and single-ended LNA is proposed to reduce insertion loss in both modes and die area. Fabricated in 65-nm bulk CMOS, the presented FEM achieves an 18.1–20 dBm output 1-dB compression point ($OP_{1\text{-}dB}$) and 24.4–33.6% peak power-added efficiency (PAE) in transmitter (TX) mode, and a 4.8–5.6 dB noise figure (NF) while consuming 5.8 mW in receiver (RX) mode, including the impact of the antenna switch.

Mo4B-3 16:20

A 5.2~7.8GHz Cryo-CMOS LNA with 4-K Noise Temperature with Cascode g_m-Boosting and Current Reuse for Noise Reduction

Yujie Geng[1], Hang Fu[2], Haotian Chen[1], Cheng Wang[1]; [1]UESTC, China, [2]Chengdu Data Automation System Technologies, China

Abstract: Fidelity of quantum state discrimination is limited by the noise temperature of cryogenic low noise amplifier (LNA), due to the temp.-independent shot noise, thermal noise due to device self-heating, and noise-impedance mismatch. This work presents a 5.2~7.8 GHz cryo-CMOS LNA, exploring the noise boundary of CMOS technology at 4.2 K. For the 1st-stage cascode device, the size (240 μm/60 nm) and current density (~44 μA/μm) are optimized for low Fano factor (F) of shot noise and high transconductance g_m. Since high transconductance efficiency g_m^2/I_D leads to low noise, a transformer-based g_m-boosting circuit enhances the g_m by 3×. In addition, the current of the 1st-stage cascode device and the 2nd-stage common source MOSFET is reused, reducing the device self-heating. Furthermore, a high-Q, off-chip inductor is used to address the noise mismatch issue. Measured at 4.2 K, the LNA attains a peak RF gain of 38 dB with a 3 dB bandwidth of 5.2~7.8 GHz. A minimum noise temperature T_e of 4 K is recorded at 6.25 GHz with a DC power P_{DC} of 10.6 mW. With a core area of 0.23 mm^2, a figure-of-the-merit (FoM_1) of 101.3 is achieved.

Mo4B-4 16:40

A 10–19.2GHz LNA Using a Partially Three-Winding Transformer and Class-AB Operation Achieving -5.3 to -2.4 dBm IP1dB for 6G FR3 Receivers

Min-Seok Baek[1], Joon-Hyung Kim[1], Jae-Hyeok Song[1], Jong-Seong Park[1], Ilhun Kim[1], Eun-Gyu Lee[1], Seong-Mo Moon[2], Dong-Pil Chang[2], Choul-Young Kim[1]; [1]Chungnam National University, Korea, [2]ETRI, Korea

Abstract: This paper presents a 10–19.2 GHz wideband low-noise amplifier (LNA) that achieves enhanced linearity and low noise by employing a partially three-winding transformer and a differential Class-AB output stage. The partially three-winding transformer in the first stage provides wideband input matching and gain boosting, enabling a low noise figure without relying on resistive feedback. The differential Class-AB second stage improves voltage swing capability and enhances large-signal behavior, resulting in higher IP1dB and robust blocker tolerance across the operating band. The proposed LNA is implemented in a 65-nm CMOS technology as a two-stage architecture. Measurement results demonstrate a 3-dB bandwidth of 10–19.2 GHz, a peak gain of 16.3 dB, a minimum noise figure of 2.13 dB, and a consistent IP1dB ranging from -5.3 to -2.4 dBm while consuming 13 mW from a 1-V supply. The design occupies a compact core area of 0.12 mm^2.

Mo4B-5 17:00

A 77.3-GHz 3.36-dB NF LNA with Cross-Coupled Noise Cancellation and Low-Loss Input Matching Transformer in 22-nm CMOS

Juncheng Deng[1], Aodi Li[1], Binzhi Liao[1], Zhongjun Zhang[1], Shaoqi Yang[1], Jing Liu[2], Zhongguang Xu[2], Robert Bogdan Staszewski[3], Liheng Lou[1], Yizhe Hu[1]; [1]USTC, China, [2]Hefei SCMI, China, [3]University College Dublin, Ireland

Abstract: This paper presents a 77-GHz low-noise amplifier (LNA) for automotive radar. The proposed front-end employs a hybrid common-source/common-gate (CS/CG) first stage with cross-coupled noise cancellation (CC-NC), achieving low input impedance (Z_{in}), intrinsic noise suppression, and enhanced effective transconductance (G_m). The reduced input impedance enables a 1:1 transformer (XFMR)-based input matching network (IMN), which provides a higher coupling coefficient and quality factor than conventional 1:2 implementations, mitigating insertion loss (IL). The subsequent stages employ neutralization and inductive degeneration to realize simultaneous noise and power matching while maintaining high gain and robust stability. Fabricated in 22-nm bulk CMOS, the prototype achieves a peak gain of 26.2 dB at 77.3GHz with a 4.6-GHz bandwidth. It attains a minimum measured noise figure (NF) of 3.36 dB at 76 GHz while consuming 18.6mW from a 0.9-V supply, demonstrating state-of-the-art noise performance among bulk-CMOS millimeter-wave LNAs.

Monday 8 June 2026
15:40–17:20
Room 257AB
Session Mo4C: Sub-THz Power Amplifiers and Bidirectional Amplifiers
Chair: Mohamed Elkhouly, Broadcom, USA
Co-Chair: Wooram Lee, Penn State, USA

Mo4C-1 15:40
A 187–224-GHz 20-dB-Gain 4.5-dBm-P_{sat} Power Amplifier with Dual-Band Matching Networks and Slotline Combining in 40-nm CMOS

Cheng-Xuan Tsai, Chun-Hsing Li; National Taiwan University, Taiwan

Abstract: A CMOS power amplifier (PA) optimized for high gain, high-power, and broadband operation is proposed for sub-THz radar applications. The transistor layout is optimized to enhance both maximum oscillation frequency (f_{max}) and output power. An interstage matching network based on a modified transformer T-model is proposed to achieve a dual-band response. Moreover, a slotline-based power divider/combiner with greater design freedom is proposed to facilitate broadband impedance matching and power division/combination. By integrating the dual-band impedance matching networks with the single-band power divider/combiner, the PA achieves broadband operation, effectively alleviating the gain-bandwidth trade-off near f_{max}. Fabricated in a 40-nm CMOS technology, the proposed PA achieves a measured 20-dB gain and a saturated output power of 4.5 dBm at 194 GHz, with a 6-dB bandwidth of 187–224 GHz. To the best of the authors' knowledge, this work demonstrates the broadest reported bandwidth for a CMOS PA operating beyond 200 GHz.

Mo4C-2 16:00
A Compact 125–150-GHz Power Amplifier in 90-nm SiGe 9HP+ BiCMOS with 34-dB Gain for Phased-Array Transmitters

Joon-Hyung Kim[1], Jae-Hyeok Song[1], Min-Seok Baek[1], Jong-Seong Park[1], Gabriel M. Rebeiz[2], Choul-Young Kim[1]; [1]Chungnam National University, Korea, [2]University of California, San Diego, USA

Abstract: This paper presents a compact, high-gain D-band PA for phased-array transmitters in a 90-nm SiGe BiCMOS (9HP+) technology. Unlike prior D-band PAs that rely on multi-way power combining, this work demonstrates that a carefully optimized single-way architecture can achieve competitive output power while maximizing gain and area efficiency under the half-wavelength pitch constraint. The PA adopts a differential three-stage architecture with broadband input/output baluns for common-mode suppression, while low-loss inductor-based inter-stage networks are employed to enhance gain and bandwidth. To mitigate substrate-related loading at mm-wave frequencies, the sub-collector (subc) termination is optimized using a high-resistance tie, improving the load-pull optimum and peak performance. Measurements show peak gain of 34 dB with 3-dB bandwidth of 25 GHz (125–150 GHz). The PA achieves a measured P_{sat} of 13.3–15.8 dBm and a peak PAE of 7.5–11% at 120–150 GHz, while maintaining a compact footprint suitable for half-wavelength antenna pitch at 140 GHz.

Mo4C-3 16:20

A 286-GHz CMOS Amplifier Achieving 56-GHz BW_{3dB} Via f_{max}-Boosting and Gain-Staggering

Dawei Tang[1], Yu-Chen Xue[1], Peigen Zhou[1], Zhe Chen[1], Jixin Chen[1], Hao Gao[2], Wei Hong[1]; [1]Southeast University, China, [2]Purple Mountain Laboratories, China

Abstract: This paper presents a 286-GHz wideband amplifier implemented in a 28-nm CMOS process. To overcome the inherent maximum oscillation frequency (fmax) limitation of the process, a custom-designed NMOS layout is proposed, boosting the fmax from 378 to 415 GHz by minimizing gate resistance and implementing an optimized vertical drain routing scheme. A 16-stage differential amplifier, leveraging a stagger-tuned matching network based on transformers, is designed to realize a flat and wideband gain response. Measurement results demonstrate a peak gain of 18 dB, a saturated output power of 2 dBm, and a recorded 3-dB bandwidth of 56 GHz spanning 230 to 286 GHz. To the authors' knowledge, this is the first reported 300-GHz-band amplifier in 28-nm CMOS, paving the way for fully integrated terahertz system-on-chips in deep-submicron CMOS processes.

Mo4C-4 16:40

A D-Band Bidirectional Amplifier Utilizing Lossy U-Boosting Network

Sunghwan Park, Yudai Yamazaki, Chenxin Liu, Chun Wang, Hiroyuki Sakai, Kazuaki Kunihiro, Kenichi Okada; Science Tokyo, Japan

Abstract: This paper proposes a D-band bidirectional amplifier using a lossy U-boosting network with off-state transistors, embedded inductors, and a Wheatstone-bridge-like feedback network to enhance Mason's invariant while increasing MAG/MSG. When the boosted Mason's invariant becomes negative, conventional gain-plane optimization is ineffective. To address this limitation, a ν-plane is introduced that remains valid for any magnitude/sign of U and whose trajectory is directly inferred from circuit parameters without approximation.

Monday 8 June 2026
15:40–17:20
Room 253ABC
Session Mo4D: Broadband and Bi-Directional Phase Shifters for RF and mm-Wave Arrays

Chair: Hao Gao, Southeast University, China
Co-Chair: Kwang-Jin Koh, Boeing, USA

Mo4D-1 15:40

A Broadband 360° Distributed Vector-Summing Phase Shifter Achieving <1.99°/0.22-dB RMS Gain and Phase Error Over 8-to-110-GHz Bandwidth

Lianbo Liu[1], Yidong Fang[1], Zhaojing Fu[1], Hao Guo[2], Taiyun Chi[2], Sensen Li[1]; [1]University of Texas at Austin, USA, [2]Rice University, USA

Abstract: This paper presents an ultra-broadband distributed vector-summing phase shifter (VS-PS) with fine resolution and full field of view over more than a decade of bandwidth. The design consists of optimally weighted distributed variable gain amplifiers (VGAs) and a three-stage polyphase quadrature hybrid network. An optimal weighting distribution is introduced, in which larger VGA cores (×4 and ×8) are divided into smaller units (×2) to improve gain and phase matching without increasing area. This approach enhances robustness against process variations and further extends the bandwidth. The impedance-invariant VGA maintains constant input and output impedances across all 1024 states, ensuring good interface matching (S_{11} and S_{22}) up to beyond 100 GHz. Furthermore, the inherent load-invariant property of the broadband, multi-stage, transformer-based I/Q hybrid tolerates large load variations (10–80 Ω) while maintaining phase and amplitude mismatches within 3° and 1 dB, respectively, across an entire decade of bandwidth. Fabricated in 22-nm FDSOI CMOS, the prototype achieves phase shifting from 8 GHz to 110 GHz, with a fine phase resolution of 3°, low RMS gain and phase errors of <0.22 dB and <1.99°, and a power consumption of only 13 mW.

Mo4D-2 16:00

A 91–125GHz 6-Bit RF Beamforming Receive Channel Using a Dual Current-Steering Phase Shifter with a Digitized Transistor Core and Tunable Gate Bias in 22-nm FD-SOI

Haisu Ju, Yingtao Zou, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a 91–125 GHz radio frequency (RF) beamforming receive channel fabricated in 22-nm CMOS fully depleted silicon-on-insulator (FD-SOI) technology. The channel consists of a wideband low-noise amplifier (LNA) and a phase shifter (PS) with 2 modes. The PS is based on dual current-steering variable-gain amplifiers (VGAs) with digitized common-gate (CG) transistor arrays and tunable CG gate bias. In PS 5-bit digital-mode, the channel achieves 0.16–0.65 dB root-mean-square (RMS) gain error and 0.67°–4.2° RMS phase error over the full bandwidth. In

PS 6-bit hybrid-mode, the RMS gain and phase errors are reduced to 0.1–0.4 dB and 0.5°–2.6°. The channel achieves a peak gain of 22 dB with a 3-dB bandwidth of 91–125 GHz, a noise figure (NF) of 6–7.8 dB and an input 1-dB compression point (IP1dB) of -31 to -25.6 dBm while consuming 77 mW of DC power, making it well suited for 6G sub-THz applications.

Mo4D-3 16:20

A 28-GHz Bi-Directional Reflection-Amplifier-Based Phase Shifter for Active Reconfigurable Intelligent Surface (RIS)

Patchara Sawakewang[1], Apisak Worapishet[2], Tissana Kijsanayotin[3], Pingda Guan[1], Chawin Khongprasongiri[1], Robert Bogdan Staszewski[1], Teerachot Siriburanon[1]; [1]University College Dublin, Ireland, [2]Mahanakorn University of Technology, Thailand, [3]Qorvo, USA

Abstract: This paper presents a low-power, bi-directional reflection-amplifier-based phase shifter (RAPS) for 28 GHz active reconfigurable intelligent surfaces (RIS). The architecture integrates a 90° hybrid coupler with an active reflection load consisting of a reflection amplifier and a 3-stage switched-filter phase shifter. By leveraging the bi-directional nature of reflection-type topologies, the proposed RAPS provides a full 360° tuning range with <0.6 dB gain variation. The prototype consumes only 5.6mW from a 0.35V supply, representing a significant advancement in power efficiency for large-scale 6G active RIS deployments.

Mo4D-4 16:40

An 8–28GHz Bidirectional Variable-Gain Phase Shifter for 6G FR3/ 5G n258 FR2 Featuring a Magnitude-Equalized Self-Similar 90° Coupler and a Simultaneously Phase-Temperature Compensated Attenuator

Basem Abdelaziz Abdelmagid, Hua Wang; ETH Zürich, Switzerland

Abstract: This work proposes a bidirectional vector modulator-based all-passive variable-gain phase shifter (VGPS) across 8–28 GHz for 6G FR3 and 5G n258 FR2. It achieves the full 360° phase shift (PS) range with a 5-bit resolution, and an 8-dB variable gain (VG) range with a 4-bit resolution. To cover this wide fractional bandwidth (FBW) with a reasonable chip size, a wideband self-similar transformer (TF)-based 90° coupler with magnitude equalization networks is proposed and utilized for the in-phase/quadrature (I/Q) generation network. Further, to achieve orthogonal and in-dB calibration-free gain control with temperature robustness, a simultaneously phase-temperature compensated switched-type attenuator is proposed and utilized for the VG units of the vector modulator-based VGPS. The design is implemented in GlobalFoundries 22nm CMOS FD-SOI with a core area of 0.43 mm^2. In the PS mode, the RMS phase and magnitude errors are lower than 3.7° and 0.74 dB across the entire band, while in the VG mode, the RMS errors are lower than 1.4° and 0.29 dB across the band.

Mo4D-5 17:00

A 24–30GHz 7-Bit Passive Hybrid Phase Shifter with <1.1° RMS Phase Error and <0.61dB Amplitude Error

Ziang Zhang, Qin Chen, Xuhao Jiang, Yuchen Liang, Xuanxuan Yang, Rui Cao, Xiangning Fan, Lianming Li; Southeast University, China

Abstract: This paper presents a 24–30 GHz 7-bit passive hybrid phase shifter with low rms phase and amplitude error, which consists of a vector-modulated phase shifter (VMPS) and a 1-bit switch-type phase shifter (STPS). A novel phase range partitioning method is proposed to reduce phase errors without the need for time-consuming and complicated calibration. To minimize the amplitude error for different phase states, a compact capacitive-compensation STPS is introduced. Fabricated with a 65nm bulk CMOS process, the proposed passive hybrid phase shifter has a core chip area of merely 0.118mm^2. Only 7-bit control bits are used to achieve the 360° phase shifting range and 5.625° phase resolution. The measurement results show that the proposed passive hybrid phase shifter achieves <1.1°/<0.61 dB RMS phase/amplitude error, respectively. At 24 GHz, the measured input 1-dB compression point (IP1dB) exceeds 15 dBm.

Tuesday 9 June 2026
08:00–09:40
Room 252AB
Session Tu1A: mm-Wave FMCW Radars and UWB Transceivers
Chair: Giuseppe Gramegna, imec, Belgium
Co-Chair: Vito Giannini, OLIX Computing, USA

Tu1A-1 08:00
A 76–81GHz FMCW MIMO Coded Transceiver for Automotive Radar
Benny Sheinman, Tom Heller, Jakob Vovnoboy, Dan Corcos, Yanir Schwartz, Michael Grubman, Dror Malowany, Yaal Horesh, Florian Bohn, Nico Bochmann, Mohamed Hussein Eissa, Iskender Haydaroglu, Stefan Malz, Chris Menkus, Robert Kim, Abhilash Nagabhushana, Ichiro Aoki, Scott Kee, Jeff Zachan, Oded Katz; indie, USA

Abstract: A 76–81 GHz FMCW automotive radar transceiver is presented, implemented in 22 nm CMOS-FDX. Its key features are four TX channels with 7-bit phase rotator delivering controllable output power up to +15 dBm, eight RX channels that support MIMO phase modulation and exhibit 9.5 dB noise figure, a dual-loop fractional-N PLL FMCW synthesizer with -96.4 dBc/Hz phase noise and built-in self-test for functional safety. The 4×4 mm^2 chip consumes 1.8 W in Time-Division Multiplexing (TDM) mode.

Tu1A-2 08:20
A Built-In Self-Test System for 60GHz MIMO FMCW Radar SoCs
Wen Zhou[1], Gennady Feygin[1], Pranav Dayal[1], Hou-Shin Chen[1], Sowmya Srinivasa[1], Renu Krishna Gutta[1], Pankaj D. Solanki[1], Gregory Rogers[1], Oren E. Eliezer[1], Mingyuan Li[1], Sai Krishna Rayudu[1], Taewoo Yu[2], Junseuk Suh[2], Joonhoi Hur[1]; [1]Samsung, USA, [2]Samsung, Korea

Abstract: This work presents a built-in self-test (BIST) system designed for a 60GHz MIMO FMCW radar SoC. Compared to conventional mmWave RFIC/module level tests which require expensive test equipment and extensive time for test system calibration and settling, on-chip BIST system reduces both the cost and time, and provides additional characterization and monitoring capabilities. In this work, we introduce a comprehensive BIST system solution that includes the co-design of hardware, test procedures and algorithms, along with the detailed breakdown of key test and calibration items.

Tu1A-3 08:40

A 28-nm FD-SOI 77-GHz Automotive FMCW Radar with Antenna Launcher in Package

Faisal Ahmed[1], Muhammad Furqan[1], Farshad Piri[1], Ibrahim Petricli[2], Mahmoud M. Pirbazari[2], Federico Vecchi[2], Chandrajit Debnath[3], Andrea Manzoni[2], A. Michelin Salomon[2]; [1]STMicroelectronics, Austria, [2]STMicroelectronics, Italy, [3]STMicroelectronics, India

Abstract: This paper presents a 77-GHz FMCW automotive radar transceiver implemented in 28-nm FD-SOI technology. The transceiver integrates a single-channel transmitter, a single-channel receiver, and a frequency multiplier chain to enable high-performance radar operation, with a PA delivering 24% peak PAE at 17.5dBm output power and an RX achieving 8.5 dB NF and +16dBm IIP_3 at chip level. The chip is packaged in flip-chip ball grid array technology and features a direct, compact transition from the MMIC to a waveguide antenna mounted on the back side of the PCB, enabling efficient RF front-end integration. The transceiver targets automotive quality and functional safety requirements and has been characterized across process corners, supply voltages, and temperature variations. Characterization includes on-wafer, on-package, and extensive radar application measurements, collectively demonstrating significant improvements over contemporary automotive radar transceivers.

Tu1A-4 09:00

An Area-Efficient NBA-MMS UWB Receiver with Capacitance Boosting and PVT-Robust RSSI for IEEE 802.15.4ab

Sumin Kang, Junhyeong Kim, Sinyoung Kim, Wonjun Jung, Jonghoon Myeong, Duyong Seo, Hyun-Gi Seok, Hyun-Chul Park, Chan-Hong Park, Joonsuk Kim; Samsung, Korea

Abstract: A reconfigurable UWB receiver supporting the IEEE 802.15.4ab narrowband-assisted multi-millisecond (NBA-MMS) ranging scheme is presented. To minimize the area overhead of NB support, a current-amplification-based capacitance-boosting (CBST) technique is proposed, achieving 49% baseband area reduction with only 0.025 mm^2 for both I and Q paths. In addition, a PVT-robust RSSI based on a mismatch-cancellation amplifier (MCA) enables reliable NB-to-UWB gain setting, achieving ± 0.5 dB nominal accuracy and within ± 1.9 dB across PVT variations. The receiver supports both NB and UWB operation while consuming 78.3 mW and occupying 0.52 mm^2.

Tu1A-5 09:20

An 802.15.4ab Narrowband Assistance RX Resilient to -32dBm Blocker at 3.2dB NF with High Dynamic Range TIA and Clip Detector

Anoop Narayan Bhat, Aasish Boora, Kaijie Ding, Johan van den Heuvel, Murat Eskiyerli, Erwin Allebes, Peng Zhang, Mario Konijnenburg, Yao-Hong Liu, Peter Vis, Christian Bachmann; imec, The Netherlands

Abstract: Encouraged by the proliferation of the 802.15.4a/z IR-UWB standard, the next generation, the 802.15.4ab, aims to extend the ranging distance by including a provision for narrowband radio assistance. Such a narrowband RX needs to achieve ~3dB NF while co-existing with WiFi blockers. We propose a 2nd-order TIA and a high dynamic range clip detector for the narrowband RX, achieving 9dB higher dynamic range than the state-of-the-art at a comparable NF and 2.5× the RF operating frequency. RX realized on a 22nm CMOS node consumes <6mW.

Tuesday 9 June 2026
08:00–09:40
Room 254AB
Session Tu1B: Frequency Multipliers from D-Band to Sub-THz
Chair: Minoru Fujishima, Hiroshima University, Japan
Co-Chair: Wei Deng, Tsinghua University, China

Tu1B-1 08:00
A Calibration-Free 55-to-70dBc H1 Rejection, 13.8% Efficiency, 102-to-120GHz CMOS Frequency Tripler Using Phase-Alignment Technique for Harmonic Recombination

Sarah Koop-Brinkmann, Victor Lasserre, Vadim Issakov; Technische Universität Braunschweig, Germany

Abstract: This paper presents a frequency tripler employing a phase-alignment-based harmonic recombination technique. By applying replicas of the input signal shifted by specific phase offsets, the unwanted harmonics are inherently canceled, while the wanted 3rd harmonic is enhanced. The circuit is realized in 22 nm FDSOI CMOS and operates from 102 to 120 GHz. Owing to the proposed technique, the design achieves a measured H1 rejection of 55 to 70 dBc over the entire operating bandwidth. As well, the circuit exhibits a peak efficiency of 13.8% and a peak output power of 8.2 dBm at 115 GHz.

Tu1B-2 08:20
A 110–142-GHz Frequency Quadrupler with 13.1-dBm P_{sat} Achieved by Coupled-Line-Based Output Matching Technique in 130-nm SiGe

Zuojun Wang[1], Haorui Luo[2], Qin Dong[2], Zhou Shu[3], Jixin Chen[4], Kevin Tshun Chuan Chai[5], Yongxin Guo[1]; [1]CityUHK, China, [2]NUS, Singapore, [3]Xidian University, China, [4]Southeast University, China, [5]A*STAR, Singapore

Abstract: This paper presents the design and measurement of a SiGe D-band frequency quadrupler, which is composed of two push-push frequency doublers (FDs) and an inter-stage driver amplifier. The simulation results indicate that implementing a purely inductive load impedance at the fundamental frequency of the FD can significantly enhance the output power. We propose a coupled-line-based output matching technique that simultaneously realizes the optimal fundamental and second harmonic load impedances for the output-stage FD. The measurement results of the fabricated quadrupler chip demonstrate a peak saturated output power of 13.1 dBm and a 3-dB bandwidth of 110–142 GHz, while the peak and saturated conversion gains reach 17.2 and 13.3 dB, respectively.

Tu1B-3 08:40

A 108–170-GHz ×6 Amplifier-Multiplier Chain with 16-dBm Output Power and >29.5-dBc Harmonics Rejection in 130-nm SiGe Process

Chang Shu[1], Lingzheng Kong[1], Peigen Zhou[1], Dawei Tang[1], Zekun Li[2], Liqun Lu[1], Jixin Chen[1], Wei Hong[1]; [1]Southeast University, China, [2]Sanechips Technology, China

Abstract: This paper presents a broadband ×6 amplifier-multiplier chain (AMC) implemented in a 130-nm SiGe BiCMOS process, comprising a differential tripler-driver amplifier, a push-push doubler, and a 95–185GHz power amplifier (PA). A three-conductor coupling-line-based reverse-side grounded balun is proposed to achieve wideband single-ended-to-differential conversion with high common-mode rejection. To ensure stable operation and broadband harmonics suppression, a stability-enhanced tripler core and hybrid high-order harmonic-rejection matching networks are developed. In addition, a compact 2-way PA with broadband staggered matching is employed to deliver a highly flat, high-power output. The fabricated AMC achieves a measured 3-dB bandwidth of 62 GHz (108–170GHz), a record peak output power of 16 dBm, and harmonics rejection exceeding 29.5 dBc. The AMC has a footprint of 0.98×2.02 mm^2, with a total DC power consumption of 1100 mW. This high-performance design is well-suited for broadband signal sources in D-band communication and microwave measurement systems.

Tu1B-4 09:00

A Broadband 241–306GHz Frequency Multiply-by-24 Based Coherent Radiator Delivering +26.5dBm EIRP in 90-nm SiGe BiCMOS

Jaskirat Singh Virdi, Wei Sun, Aydin Babakhani; University of California, Los Angeles, USA

Abstract: This work presents a fully-integrated 241–306 GHz coherent radiator for the 300 GHz band. Integrated with an on-chip dipole antenna, the proposed radiator utilizes a frequency multiply-by-24 chain (FMC) to upconvert a low-frequency LO input to the 300 GHz band. The FMC is realized using a cascade of three push-push frequency doublers, followed by a differential 300 GHz frequency tripler. A radiator prototype is implemented in GlobalFoundries 90-nm SiGe BiCMOS, and free-space chip measurements are shown. Consuming 148 mW DC power, the prototype demonstrates state-of-the-art 29.6% tuning range, peak EIRP of +26.5 dBm (with lens) at 267 GHz, 6-dB bandwidth of 241–306 GHz, and 1.2% DC-to-THz efficiency. Harmonic spectral purity is characterized, and the prototype demonstrates 26.5 dBc mid-band harmonic rejection. The proposed radiator is integrated with a 24× FMC, covers most of the 300 GHz band and demonstrates state-of-the-art tuning range and EIRP.

Tuesday 9 June 2026
08:00–09:40
Room 257AB
Session Tu1C: Scalable, Calibrated mm-Wave and Wideband Tx/Rx Front-Ends for Radar, 5G, and SATCOM

Chair: Emanuel Cohen, Technion, Israel

Co-Chair: Khaled Khalaf, Pharrics, Belgium

Tu1C-1 08:00

A 2–18GHz Integrated 4-Channel Transmit/Receive Beamformer in 65-nm CMOS

Jianhao Gong, Yudi Yang, Kun Gao, Zixuan Wang, Xingcun Li, Zan Zhou, Jiewen Wang, Huibo Wu, Wenhua Chen; Tsinghua University, China

Abstract: This paper presents an ultra-wideband integrated phased-array beamformer chip integrating 4 transmit/receive (TRX) channels in 65-nm CMOS process. Each channel features 16.2 dB TX gain over a 12:1 3-dB bandwidth from 1.5 GHz to 18.1 GHz, and 16.3 dB RX gain over a 9:1 3-dB bandwidth from 1.9 GHz to 18 GHz, respectively. By employing vector modulation scheme for phase shifting and designing an impedance-invariant variable gain amplifier (IIVGA), the chip provides 6-bit phase control and 20 dB gain control for both transmit and receive modes. To the best of our knowledge, this work achieves the widest operating bandwidth among TRX beamformers for applications in wideband radars and wireless communication systems.

Tu1C-2 08:20

A K-Band 4-Beam Phased Array Transmitter in Only 5-Layer PCB Enabled by Silicon-Assisted Beam-Combining Network for SATCOM

Ruiyang Jiang, Haikun Jia, Huanyu Ge, Jiankai Zhao, Wei Deng, Baoyong Chi; Tsinghua University, China

Abstract: Conventional fully-connected multi-beam phased arrays (FC-MBPA) face severe integration challenges due to complex beam-combining networks (BCN), leading to high complexity and over 10 PCB metal layers. To address this, we propose a scalable silicon-assisted architecture. A 16-to-4 beam-combining chip with high isolation is developed in 65-nm CMOS process, which can be switched to K- or Ka-band. As a proof of concept, a K-band 4-beam 16-element transmitter in only 5-layer PCB is presented. The prototype achieves ±30° beam scanning, <-31.6 dB inter-beam coupling and >17.1 dB cross-polarization discrimination (XPD). The array can also deliver 45.5 dBm maximum EIRP and 200-MSps 16-QAM signal with 3.56% EVM. With >60% reduction in PCB thickness, the proposed architecture lowers system complexity and antenna feeding loss, offering a cost-effective solution for scalable SATCOM systems with 4 beams and beyond.

Tu1C-3 08:40

Scalable and Compact Fully-Connected Network Based on Gm-Cell Grid for 28-GHz Multi-Stream MIMO Receiver

Seunghoon Lee[1], Sungmin Cho[1], Seung-Uk Choi[1], Sungbeom Kim[2], Inho Choi[1], Jiwon Kang[1], Youngseo Du[1], Ho-Jin Song[1]; [1]POSTECH, Korea, [2]Samsung, Korea

Abstract: This paper presents a scalable and compact 28-GHz 4-element 4-stream CMOS fully-connected receiver designed for multi-beam multiple-input multiple-output (MB-MIMO) operation, where high beam-to-beam (B2B) isolation enables concurrent in-band communication. To overcome the scalability and crosstalk issues of conventional architectures, a 2D Gm-cell grid-based network is implemented. This design employs variable-gain phase shifters with a current-bleeding technique to maintain constant output impedance, while differential input/output lines are utilized to suppress capacitive crosstalk, achieving over 25 dB of B2B isolation. The fabricated chip occupies 5.33 mm^2 and demonstrates a total data rate of 6.4 Gb/s in a 4-stream MB-MIMO over-the-air test using four different modulation schemes. Notably, the fully connected network occupies only 3.49% of the total core area, highlighting exceptional area efficiency. Overall, the proposed architecture provides a compact yet high-performance solution for scalable MB-MIMO receivers, achieving superior B2B isolation and robust multi-stream operation.

Tu1C-4 09:00

A 256-Element 28GHz 5G NR Wirelessly-Powered Active Relay Transceiver with TDD Synchronization Free Bidirectional Amplifiers

Shu Date, Atsuya Hirayama, Sena Kato, Keito Yuasa, Michihiro Ide, Masayuki Kikuchi, Takashi Tomura, Jill Mayeda, Atsushi Shirane; Science Tokyo, Japan

Abstract: In this paper, we propose a millimeter-wave relay system powered entirely by energy harvested by wireless power transfer (WPT), eliminating the need for TDD synchronization. The relay transceiver uses a TDD synchronization free bidirectional amplifier, allowing the system to continuously receive and transmit signals without T/R switches or TDD synchronization signals. This combined with the transceiver being fully powered by received WPT signals, which removes the need for external power supply units, reduces the system installation complexity. The bidirectional amplifier consists of two Wilkinson dividers and amplifiers that perform simultaneous two-way amplification. The prototype IC integrates an unequal bidirectional amplifier that uses unequal Wilkinson dividers to improve the noise figure. The prototype IC has 16 paths per chip, and the prototype board is a 256-element transceiver. The proposed relay transceiver supports 256QAM for the Rx and 64QAM for the Tx with a 400MHz bandwidth, standard compliant 5G NR OFDMA-mode modulated signals.

Tu1C-5 09:20

A W-Band FMCW Radar Transceiver with Self-Calibrated Type-III ADPLL Achieving 1.27-cm Range Resolution for Imaging Applications

Ling Hao, Haoyu Bai, Zhenkun Shen, Ningyuan Zhang, Jiazheng Zhou, Chuancheng Wu, Zihe Wang, Junhua Liu, Huailin Liao; Peking University, China

Abstract: This paper presents a W-band frequency-modulated continuous wave (FMCW) radar transceiver designed for centimeter-level imaging applications. The transceiver features a self-calibrated Type-III all-digital phase-locked loop (ADPLL) that generates highly linear wideband chirps by correcting both band-transition discontinuities and slope errors through LMS-based adaptive overlap compensation and Type-III ramp-tracking control. To enable precise beam steering without extra path loss, a 19-bit equivalent phase shifting capability is embedded directly within the fractional-N division path. The transmitter (TX) delivers 11 dBm saturated output power, and the receiver (RX) provides 30 dB gain with a minimum noise figure (NF) of 8.66 dB. Measurements demonstrate a 12-GHz chirp bandwidth with an RMS frequency error of only 48.7 kHz. Over-the-air (OTA) experiments with a corner reflector validate a range resolution of 1.27 cm. Implemented in a 40-nm CMOS process, the chip occupies 1.35×2.43 mm^2 and consumes 270 mW.

Tuesday 9 June 2026
08:00–09:40
Room 255
Session Tu1J: High-Speed Optical Transceivers
Chair: Sajjad Moazeni, University of Washington, USA
Co-Chair: Subhanshu Gupta, Washington State University, USA

Tu1J-1 08:00
A 460Gb/s PAM-4 Linear Distributed Driver with 105GHz BW for TFLN Modulators in 130nm SiGe BiCMOS

Leandro da Silva[1], Cedric Bruynsteen[1], Jakob Declercq[1], Armands Ostrovskis[2], Fabio Pittala[2], Guy Torfs[1], Nishant Singh[1], Xin Yin[1]; [1]Ghent University, Belgium, [2]Keysight Technologies, Germany

Abstract: We present a linear single-ended distributed driver implemented in 130nm BiCMOS process with f_T / f_{max} of 470/650 GHz, designed for single-ended push-pull thin-film lithium niobate (TFLN) traveling-wave Mach-Zehnder modulators (TW-MZMs). High-linearity and low group-delay variation are achieved by using 10 cascode gain cells with large emitter degeneration resistors (23.5 Ω) and no capacitive peaking. The driver delivers an overall gain of 14.5 dB, a bandwidth of 105.7 GHz, and an output swing of 2.25 Vpp. Time domain experiments demonstrate 232 Gbaud PAM-4 (464 Gbps gross aggregate rate) with the use of offline DSP.

Tu1J-2 08:20
A 200-Gb/s Low-Noise TIA in 28-nm CMOS

Feiyang Zhang[1], Jianyu Yang[1], Yifei Xia[1], Zhixing Zhang[1], Ruixuan Yang[1], Liang Zhao[1], Wenxin Zhang[1], Cailing Li[1], Zetong Zhang[1], Shenlei Bao[2], Binhao Wang[2], Li Geng[1], Dan Li[1]; [1]Xi'an Jiaotong University, China, [2]CAS, China

Abstract: This paper presents a 200-Gb/s low-noise transimpedance amplifier (TIA) implemented in standard 28-nm CMOS technology, addressing the escalating bandwidth demands of artificial intelligence data centers (AIDCs). The proposed TIA employs a three-stage front-end with a inductive peaking strategy, a single-to-differential equalizer (S2D-EQ), and a linear CML output buffer for signal performance. The TIA achieves transimpedance gain of 61.6 dBΩ, an O-E bandwidth of 48 GHz, and an input-referred noise density of 11.5 pA/√Hz while consuming 116 mW (0.58 pJ/bit). The TIA supports 100-GBaud PAM-4 modulation, validating its suitability for next-generation high-density optical communication systems.

Tu1J-3 08:40

A 4×212Gbps 3.34pJ/bit Electronic-Photonic Co-Designed Transmitter Chipset in 0.18-μm SiGe BiCMOS and 90nm Silicon Photonics

Ziyue Dang[1], Ziyu Deng[2], Ye Liu[2], Qiansheng Wang[2], Zhicheng Wang[2], Ziying Xieg[2], Ruiyang Jiang[3], Haikun Jia[3], Min Tan[1], Xi Xiao[2]; [1]HUST, China, [2]NOEIC, China, [3]Tsinghua University, China

Abstract: A 4×212 Gbps, 3.34 pJ/bit PAM-4 optical transmitter chipset for Linear Pluggable Optics (LPO) applications is presented, featuring a co-designed architecture with a 57 GHz E/O bandwidth and a 20 dB gain control range. The proposed distributed driver consists of two Distributed Variable Gain Amplifier (DVGA) stages and a Distributed Amplifier (DA) output stage, achieving an E/E bandwidth larger than 67 GHz and 3Vppd for 212 Gbps PAM-4 operation. Distributed Equalization technique is used for bandwidth extension while maintaining low group delay variation. Broadband output matching up to 60 Ohms is realized through co-design of the DA output stage with a substrate-undercut Silicon Photonics Mach-Zehnder modulator (SiPh MZM). The integrated optical transmitter chipset achieves 212 Gbps PAM-4 operation with clear eye openings, an extinction ratio (ER) of 3.62 dB, and a TDECQ of 3.69 dB.

Tu1J-4 09:00

A 55-GHz Bandwidth PAM-4 InP DHBT Photoreceiver Based on PD-TIA Co-Design for >112-GBd Optical Transceivers

Antoine Chauvet[1], Romain Hersent[1], Fabrice Blache[1], Filipe Jorge[1], Marie Da-Rocha-Amaro[1], Karim Mekhazni[1], Harry Gariah[1], Nil Davy[1], Colin Mismer[1], Virginie Nodjiadjim[1], Michel Goix[1], Agnieszka Konczykowska[1], Bertrand Ardouin[1], Christophe Caillaud[1], Abed-Elhak Kasbari[2], Achour Ouslimani[2]; [1]III-V Lab, France, [2]ENSEA-LÉA, France

Abstract: We present a photoreceiver assembly optimized through comprehensive modeling of the photodiode (PD), the transimpedance amplifier (TIA), and their interconnection. This allows an early and accurate optical signal-to-noise ratio (OSNR) prediction during the TIA design. Fabricated in a 0.5-μm InP DHBT technology, the standalone TIA achieves a 59-dBΩ transimpedance gain and a 70-GHz electrical bandwidth, supporting PAM-4 operation up to 100 GBd without digital signal processing. When wire-bonded to a 50 GHz PD, the photoreceiver exhibits a flat electro-optical response with 55 GHz of bandwidth. Open PAM-4 eye diagram is demonstrated up to 112 GBd with a 1.56 pJ/bit efficiency, using a 6-tap off-line feed-forward equalizer. High linearity is obtained, with a 1-dB gain compression point reached at 3.5 dBm input optical power, corresponding to a 650-mV electrical output swing. These results pave the way to beyond-112-GBd direct-detection optical transceivers.

Tuesday 9 June 2026
10:10–11:50
Room 252AB
Session Tu2A: Broadband RF Front-End Components for Next-Generation Wireless Systems
Chair: Bichoy Bahr, Texas Instruments, USA
Co-Chair: Justin Wu, AmLogic, USA

Tu2A-1 10:10
A 5–7GHz Channel and Bandwidth Selective Shunt N-Path LNA Based Receiver with +6dBm OOC IB1dB, <-71dBm LO Re-Radiation for WiFi 7 Multi-Link Operation

Ran Krichman[1], Ashoke Ravi[2], Natan Ershengoren[1], Rotem Banin[2], Sashank Krishnamurthy[2], Uri Grosglik[1], Oded Tal[1], Nave Sharvit[1], Oren E. Avraham[1], Sarit Zur[1], Ofir Degani[1]; [1]Intel, Israel, [2]Intel, USA

Abstract: This paper presents a fully integrated low-cost 14nm CMOS 5–7GHz 160MHz bandwidth RF to ADC Wi-Fi 7 receiver, based on a channel and bandwidth selective second order shunt N-path band pass filter LNA topology, for dual-radio wireless systems. The prototype receiver achieves up to +6dBm out-of-channel IB1dB and <-71dBm LO re-radiation.

Tu2A-2 10:30
A Single-Stage Feedback-Feedforward D-Band LNA in SiGe BiCMOS

Guglielmo De Filippi[1], Lorenzo Piotto[1], Andrea Mazzanti[2]; [1]Fondazione Chips-IT, Italy, [2]Università di Pavia, Italy

Abstract: This paper presents a compact and low-power D-band low-noise amplifier (LNA) implemented in 55 nm SiGe BiCMOS. The circuit is based on the cascode configuration, and to address the fundamental gain limitations that arise when operating near the transistor fmax and over a large fractional bandwidth, gain boosting is concurrently applied to both the common-emitter (CE) and common-base (CB) through a combination of reactive feedback and feedforward. The trade-off between gain-boosting and bandwidth is analyzed, and the amount of boosting is set to preserve broadband operation. The interstage and output matching networks keep the bandwidth by exploiting dual-resonance. The realized amplifier demonstrates 14.5dB gain over a 50-GHz bandwidth (116–166 GHz) and a minimum noise figure of 4.8 dB. The feedback network also enables dynamic DC power expansion, yielding a peak OP_{1dB} of 2.8 dBm at 12.2 mW and a record 15.5% power efficiency. Compared to prior sub-THz LNAs in similar technologies, the proposed design demonstrates 3× improvement in figure-of-merit, validating the effectiveness of the design.

Tu2A-3 10:50

A Broadband G-Band Frequency Doubler in 130-nm SiGe Technology

Mingquan Bao[1], Yu Yan[2], Klaus Aufinger[3], Herbert Zirath[2]; [1]Ericsson, Sweden, [2]Chalmers University of Technology, Sweden, [3]Infineon Technologies, Germany

Abstract: This paper presents a broadband G-band frequency doubler implemented in 130-nm SiGe BiCMOS technology. The design features an active balun integrated with a stacked doubler-and-amplification (D&A) stage. The active balun converts a single-ended input into differential fundamental signals while generating common-mode second-harmonic signals on the noninverting and inverting paths. The D&A stage, comprising three stacked common-base transistor pairs, concurrently doubles the frequency of the differential fundamental component to generate the common-mode second harmonic and amplifies the common-mode second-harmonic component from the active balun. Optimization of transistor dimensions and transmission-line lengths within the D&A stage minimizes imbalance between the noninverting and inverting paths for the fundamental signal. Consequently, the stacked topology enhances output power while improving fundamental rejection. Measurement results demonstrate a peak output power of 6.3 dBm at 180 GHz, a 3-dB bandwidth of 67 GHz (145–212 GHz, corresponding to a fractional bandwidth of 37.5%), and a peak efficiency of 2.2%. The measured fundamental rejection is greater than 20 dBc. The circuit occupies a total chip area of 0.56 mm^2 (core: 0.072 mm^2).

Tu2A-4 11:10

A Fully Differential DC-Capable RF SPDT Switch in SOI

Ilker Kalyoncu, Huseyin Kayahan; Analog Devices, Türkiye

Abstract: This paper introduces the first fully differential SOI SPDT switch with true dc switching capability combined with broadband RF performance. The design operates from dc to 12 GHz while sustaining ±8 V common-mode voltage and handling 31 dBm differential RF power. A series-shunt topology with four stacked transistors per branch is combined with distributed dc tracking loops that bootstrap gate/body resistors up to 20 MHz, overcoming the low-frequency power-handling vs switching-speed trade-off. A start-up scheme enables ±12 V supply operation in a 3.3 V process. Measured results demonstrate sub-1 dB insertion loss and excellent linearity (>34 dBm IP1dB and ~60 dBm IP3), enabling robust switching of high-speed differential links and instrumentation paths requiring mixed dc and RF capability.

Tuesday 9 June 2026
10:10–11:50
Room 254AB
Session Tu2B:
Advanced Phase-Locking and Clock Generation Techniques
Chair: Ahmed Elkholy, Broadcom, USA
Co-Chair: Wanghua Wu, Samsung, USA

Tu2B-1 10:10
An 8–28-GHz 16-Phase Delay Locked Loop Employing Nested Feedback Loops in 28-nm CMOS

Junyan Bi[1], Yechen Tian[1], Junjie Gu[1], Kaixuan Cen[1], Xiaoliang Shen[2], Hao Xu[1], Na Yan[1]; [1]Fudan University, China, [2]NICIC, China

Abstract: This work presents a 16-phase delay-locked loop operating across 8 to 28 GHz in 28 nm CMOS. The proposed two-stage nested-feedback architecture enables the DLL to overcome the frequency limit set by the minimum delay of an inverter. An AC-coupled delay-unit structure is further introduced to suppress duty-cycle variation accumulated through multi-stage signal propagation. Fabricated in a 28 nm CMOS process, the proposed design achieves an output jitter of <47 fs and a phase error of <2.5° across 8–28 GHz.

Tu2B-2 10:30
A 6.2-GHz Reference-Feedthrough-Suppressed Type-I Sampling PLL with a Bottom-Plate-Sampling PD Scoring 18.2 fs_{rms} Jitter, -258.7-dB FoM and -80.6-dBc Reference Spur

Ningyi Zhang[1], Jinhai Xiao[1], Xiaolong Liu[2], Rui Liu[1], Junao Zhu[1], Yuanhao Zhou[1], Futian Liang[3], Xinzhe Wang[3], Wenyi Peng[3], Yintang Yang[1], Xiaohua Ma[1], Yue Hao[1], Maliang Liu[1], Yong Chen[4]; [1]Xidian University, China, [2]SUSTech, China, [3]USTC, China, [4]Tsinghua University, China

Abstract: This paper presents a type-I sampling phase-locked loop (S-PLL) incorporating a bottom-plate sampling phase detector (BPS-PD). The BPS-PD eliminates the input reference to the voltage-controlled oscillator (VCO) feedthrough by clamping the sampling nodes to the constant common-mode potential, while ensuring a stable boosted phase detector gain through passive gain multiplication. Fabricated in a 28-nm CMOS process and integrated with a series-resonant VCO (SR-VCO), the S-PLL prototype achieves a state-of-the-art 18.2-fs_{rms} jitter at an operating frequency of 6.2 GHz with a reference spur of -80.6 dBc. The jitter-power figure-of-merit reaches -258.7 dB.

Tu2B-3 10:50

A 25.4fs Jitter Fractional-N Digital PLL with an LC-Based Power-Gated Oscillator and Series-Resonance DCO

Daniele Lodi Rizzini[1], Michele Rossoni[1], Filippo Osio[1], Stefano Gallucci[1], Riccardo Moleri[1], Andrea Mazzanti[2], Andrea L. Lacaita[1], Simone M. Dartizio[1], Salvatore Levantino[1]; [1]Politecnico di Milano, Italy, [2]Università di Pavia, Italy

Abstract: This work presents a 10-to-12-GHz digital PLL employing a compact series-resonance oscillator to minimize out-of-band phase noise and an LC-based power-gated oscillator to suppress in-band noise and fractional spurs. Implemented in a 55-nm BiCMOS process, the PLL achieves RMS jitter of 14.9 fs and 25.4 fs at 11 GHz integer-N and near-integer fractional-N modes, respectively, while consuming 310 mW.

Tu2B-4 11:10

A 2.4-GHz 168-fs_{rms}-Jitter and -56-dBc-Reference-Spur RO-Based Cascaded Injection-Locked Clock Multiplier

Qixuan Luo, Hongyu Mao, Xiaolong Liu; SUSTech, China

Abstract: This work presents a low-jitter, low-reference-spur ring oscillator (RO)-based cascaded injection-locked clock multiplier (ILCM). To enhance noise suppression bandwidth, the proposed cascaded ILCM integrates a reference quadrupler with a sub-harmonic injection-locked RO (SILRO). The reference quadrupler eliminates the need for additional duty-cycle calibration, while the narrow pulses generated by the quadrupler lock the SILRO, enabling a clock multiplication factor ranging from 16× to 32×. Additionally, a frequency-locking loop (FLL) and a phase-adjustment loop (PAL) are embedded within the SILRO to track the sub-harmonic injection frequency and compensate for phase deviations induced by the injection. Fabricated in a 65-nm CMOS process, the proposed prototype achieves a locking range from 1.6 to 3.2 GHz. At 2.4 GHz, the measured reference spur is -56 dBc, the RMS jitter is 167.6 fs, and the jitter figure-of-merit (FoM_{jitter}) is -246 dB at 2.4 GHz.

Tu2B-5 11:30

An Ultra Low Noise 5-GHz Ring Oscillator-Based PLL with Over-Sampling Feedforward Phase Noise Cancellation Achieving -267.05dB FoM_N

Yi-Hsiang Huang, Po-Hao Cheng, Jacques C. Rudell; University of Washington, USA

Abstract: A 5 GHz ring-oscillator-based phase-locked loop (PLL) fabricated in 28 nm CMOS achieves 198.5 fs RMS jitter (1 kHz–100 MHz), -267.05 dB normalized jitter-power figure of merit, and -247.05 dB figure of merit. An oversampling feedforward phase noise cancellation architecture with an 8-phase passive gain-boosted sampler extends the cancellation bandwidth to 10× the loop bandwidth (40 MHz at a 4 MHz loop bandwidth) while maintaining a -67.7 dBc reference spur. The PLL occupies 0.41 mm^2 and consumes 5 mW from 0.9 V/1.8 V supplies.

Tuesday 9 June 2026
10:10–11:50
Room 257AB
Session Tu2C: Next Generation Sub-THz Circuit Blocks
Chair: Vadim Issakov, Technische Universität Braunschweig, Germany
Co-Chair: Kenichi Okada, Science Tokyo, Japan

Tu2C-1 10:10
A 110–170GHz Phase-Insensitive and PVT-Robust Digital-Step Attenuator with Phase Compensation and Background Step Calibration

Basem Abdelaziz Abdelmagid, Adam Wang, Hua Wang; ETH Zürich, Switzerland

Abstract: This work proposes a low-loss digital-step attenuator (DSA) that covers the entire D-band (110–170 GHz) with a tuning range of 15.5 dB and a step of 0.5 dB. Utilizing a multi-stage reflective-type attenuator (RTA) with phase compensation per stage, the DSA simultaneously achieves high precision and low phase variations. Further, a background step-calibration loop is proposed and employed to maintain robust performance with reduced root-mean-square (RMS) and differential nonlinearity (DNL) magnitude errors across process, voltage, and temperature (PVT) variations. The design is implemented in GlobalFoundries 22nm CMOS FD-SOI, achieving a low insertion loss (IL) of 3.5 dB at the reference state at 140 GHz, which can be simply compensated by a single D-band driver stage. The measured RMS magnitude and phase errors remain below 0.19 dB and 2.7° respectively across the entire D-band.

Tu2C-2 10:30
A 121/145GHz Dual-Band LNA with Single-Path and Dual-Mode Gain-Boosting Core in 28nm CMOS

Hokeun Lee[1], Hyo-Ryeong Jeon[1], Namun Hwang[1], Sang-Gug Lee[1], Kyung-Sik Choi[2]; [1]KAIST, Korea, [2]Yonsei University, Korea

Abstract: This paper presents a low-noise amplifier (LNA) that achieves dual-band operation by employing a cascaded single-path and dual-mode gain-boosting amplifier core. The proposed LNA selectively amplifies the low band (LB) under common mode (CM) excitation and the high band (HB) under differential mode (DM) excitation. This allows nearly independent tuning per band and flexible band spacing with a shared signal path and bias condition. To realize this at D-band, a dual-mode wideband gain-boosting technique is proposed, where the embedding is reused in the CM and DM to enhance the gain at the LB and HB, respectively. In addition, a dual-mode inter-stage matching network extends the dual-mode (CM/DM) concept to a multi-stage cascaded architecture, enabling gain enhancement while sharpening the gain selectivity between the LB and HB. Implemented in a 28 nm CMOS process, the proposed LNA achieves measured peak gains of 19.9/21.9 dB with a 3 dB bandwidth of 19.8/18 GHz in the LB/HB. The measured noise figures are 8.5/8.9 dB for the LB and HB, respectively.

Tu2C-3 10:50

A 224-GHz 5.9-dBm-P_{out} VCO Utilizing Deep-Triode-Induced Current Top-Clipping Technique

Miao Yu, Jin Zhang, Kaixue Ma, Zhen Yang; Tianjin University, China

Abstract: This paper presents a high-power second-harmonic voltage-control oscillator (VCO) utilizing the deep-triode-induced current top-clipping (DT-CTC) technique. By employing a cascode topology featuring a drain-source magnetic-coupling configuration, the core transistors are periodically driven into the deep triode region. This results in significant drain current top clipping, generating a waveform with high second-harmonic content. Unlike conventional cutoff-induced harmonic-generating methods, this approach overcomes output power (P_{out}) and start-up bottlenecks. Furthermore, a quad-core coupled architecture with shared bias networks and power combining is implemented to further enhance P_{out} and improve phase noise (PN). The proposed VCO is fabricated in a 28-nm CMOS process and features a peak P_{out} of 5.9 dBm, an optimal PN of -112 dBc/Hz at a 10-MHz offset, a tuning range of 12.2% (211.4–235.7 GHz), and a peak figure of merit with a tuning range (FoM_T) of -178.2 dBc/Hz.

Tu2C-4 11:10

A 111.5GHz-to-163.6GHz 37.9%-Tuning-Range -200.3dBc/Hz-FoM_T VCO Employing Hybrid Coarse-Magnetic-Tuning and Fine-Capacitive-Tuning Techniques

Hanlin Yang, Bodong Zhang, Yi Liu, Zixi Jing, Zhiyu Liu, Howard C. Luong; HKUST, China

Abstract: A sub-THz VCO employs hybrid tuning techniques to achieve ultra-wide frequency tuning range with high Q_{tank} and low phase noise. Coarse magnetic tuning features a compact 12-section 3-layer stacked transformer exploiting only maximum Q_L points while fine capacitive tuning utilizes a 3-section customized high-Q_C MOM variable capacitors. The VCO measures 37.9% FTR from 111.5GHz to 163.6GHz and PN@10MHz offset of -114.2dBc/Hz while consuming 4.5–6.0mW, resulting in the best FoM of -188.8dBc/Hz and FoM_T of -200.3dBc/Hz.

Tu2C-5 11:30

A 220 to 260GHz Ultra-Compact, Calibration-Free 5-Bit Phase Shifter with 1.8° RMS Phase Error in 9HP SiGe Process

Meijun Tian, Liwen Zhong, Wooram Lee; Penn State, USA

Abstract: This paper presents a precise, calibration-free 220-to-260-GHz 5-bit phase shifter based on a passive trombone-like topology, implemented with reverse-saturation NPN bipolar junction transistors (BJTs). The reverse-saturation NPN BJT exhibits a significantly smaller $r_{ON}C_{OFF}$ and a higher off-state quality factor compared to the conventional forward-saturation NPN BJT, enabling the design of a low-loss, high-resolution phase shifter above 200 GHz. The prototype IC is fabricated in GlobalFoundries 9HP SiGe process and occupies only 0.033 mm^2. The phase control operates in 11.25° steps across 360° at 240 GHz, with an average insertion loss of 14 dB and a DC power consumption of 12 mW. Measurement results for 14 samples without calibration demonstrate a mean RMS phase and gain error of 1.8° and 0.74 dB at 240 GHz, respectively.

Tuesday 9 June 2026
10:10–11:50
Room 255
Session Tu2J: Co-Packaged Optics and Die-to-Die Interfaces
Chair: Zeshan Ahmad, Coherent, USA
Co-Chair: Bahar Jalali Farahani, Cisco, USA

Tu2J-1 10:10
A 1.49pJ/b 4-Channel 256-Gb/s MRM-Based Coherent Co-Packaged Optics with Linear Carrier Phase Recovery
Pengyu Zeng, Marziyeh Rezaei, Daniel Sturm, Asha Rashmi Nayak, Hongyong Li, Sajjad Moazeni; University of Washington, USA

Abstract: AI interconnect scaling requires compact, low-power, low-latency co-packaged optics (CPO). We demonstrate a 4-channel 256 Gb/s laser-forwarded coherent CPO optical link using 4-Offset-QAM modulation at 64 Gb/s per channel in 45nm GF monolithic silicon photonics process for this application. We use micro-ring modulators (MRM) with on-chip analog-based carrier phase recovery (CPR). We further introduce a negative Miller capacitor TIA bandwidth extension technique for coherent detections, improving SNR by ~5 dB without any power overhead. Measured transmitter eye diagrams show 7.9 dB ER and 5 dB IL, with 0.67 pJ/b energy-efficiency. The receiver achieves -12.3 dBm sensitivity at pre-FEC BER <1e-10 with 0.82 pJ/b.

Tu2J-2 10:30
A 200Gbps 0.67pJ/bit Transceiver Front-End for Silicon-Photonics with Group Delay and Nonlinear Adjustment in 28nm CMOS
Yihao Yang, Shenlei Bao, Chao Cheng, Binhao Wang; CAS, China

Abstract: This work presents 28nm CMOS transceiver (TRX) circuitry for 3D integration with silicon-photonic (SiPh), incorporating micro-ring modulators (MRMs) and p-i-n photodiodes (PDs) to enable high-density co-packaged optics (CPO) and optical I/O (OIO). To meet the high-speed requirements of SiPh links, a combination of over-peaking and complex zero-continuous-time linear equalizer (CZ-CTLE) is employed to extend the bandwidth of both the transmitter (TX) and receiver (RX) electrical chips, while maintaining a flat group delay variation (GDV) within the 100Gbaud's Nyquist frequency. Additionally, to mitigate the intrinsic nonlinearity of the MRM, an asymmetrically biased driver architecture is introduced to enhance the linearity of the optical transmitter (OTX). Measurement results show that the proposed TX (RX) supports 200Gbps (224Gbps) PAM4 signal transmission, achieving GDV below 2.28ps (1.47ps) within 100GBaud's Nyquist frequency, along with bandwidth densities of 2.39Tbps/mm^2 (4.9Tbps/mm^2) and a total energy efficiency of 0.67pJ/bit.

Tu2J-3 10:50

An 8×64Gb/s PAM-4 Retimed Optical Receiver with Forwarded Clock for UCIe Compliant Optical I/O in 28-nm CMOS

Yukun He[1], Junhao Zhao[1], Zhouchi Duan[1], Puxi Tan[1], Yucong Li[1], Yujie Zeng[1], Zhihao Peng[1], Huanfa Sun[1], Shangjie Wei[1], Chenming Zhang[2], Dong Wang[2], Shiming Wu[2], Jian Luan[2], Hao Luo[2], Xiaoyan Gui[1]; [1]Xi'an Jiaotong University, China, [2]Sanechips Technology, China

Abstract: This work presents an 8×64 Gb/s four-level pulse amplitude modulation (PAM-4) retimed optical receiver (ORX) with forwarded clock for universal chiplet interconnect express (UCIe) compliant optical I/O (OIO). The AFE employs a transadmittance-stage transimpedance-stage (TAS-TIS) where a dual-gain path single-to-differential (S2D) topology is proposed to enhance linearity for PAM-4 signaling. A shared forwarded optical clock (FOC) network is adopted for better jitter tracking and higher area efficiency. A two-stage high-speed slicer is proposed to realize 64 Gb/s PAM-4 signal sampling. The proposed ORX is implemented in a 28-nm CMOS process and co-packaged with a dedicated photodetector (PD) array via flipchip bonding, enabling 512 Gb/s PAM-4 aggregated data transmission with a bandwidth density of 955 Gb/s/mm^2 and an energy efficiency of 2.25 pJ/bit.

Tu2J-4 11:10

A 3.5-to-14GHz, Less-Than-0.81LSB-INL$_{pp}$, 7b Adaptive Phase Interpolator with Segment-Squeeze INL Calibration Algorithm for Die-to-Die Interfaces

Shiju Li[1], Yihan Chen[2], Wei Deng[1], Nan Qi[2], Haikun Jia[1], Liyuan Liu[2], Baoyong Chi[1]; [1]Tsinghua University, China, [2]CAS, China

Abstract: Addressing the stringent requirements for high linearity and compact footprint in die-to-die (D2D) interfaces, this paper presents a 7-bit adaptive phase interpolator (PI) employing a segment-squeeze integral nonlinearity (INL) calibration (SSIC) algorithm. Fabricated in 28nm CMOS, the design achieves automatic calibration through a multi-lane shared loop. The PI operates over a frequency range of 3.5–14GHz with a compact core area of 0.0207mm^2. Measurement results demonstrate that the peak-to-peak INL (INL$_{pp}$) is less than 0.81LSB at 14GHz, achieving state-of-the-art performance and exhibiting robust resilience against process, voltage, temperature (PVT) variations.

Tuesday 9 June 2026
13:30–15:10
Room 252AB
Session Tu3A: Recent Advances in GaN Technology
Chair: Oleh Krutko, imec, Ireland
Co-Chair: Harshpreet Bakshi, Texas Instruments, USA

Tu3A-1 13:30
High-Performance Near-Enhancement-Mode InAlGaN/GaN HEMTs on Silicon with High f_T/f_{MAX} of 71.5/173.1GHz for Millimeter-Wave Applications

Hsuan-Yao Huang[1], Po-Wei Chen[1], You-Chen Weng[1], You-Ting Lin[1], Fitriyadi[1], Jeng-Chyang Sun[2], Chen Zhang[2], Edward Yi Chang[1]; [1]NYCU, Taiwan, [2]Infinity Communication Technology, Taiwan

Abstract: An enhancement-mode recess-free InAlGaN/GaN HEMT on silicon is demonstrated for millimeter-wave RF applications by combining a polarization-engineered ultra-thin InAlGaN barrier with a high-quality LPCVD SiN_x passivation stack. The strong polarization-induced channel charge enables positive threshold voltage (V_{th}) without gate recess, while the dense LPCVD SiN_x effectively suppresses interface traps and gate leakage current. The proposed devices exhibit a high peak transconductance (g_m) of 708 mS/mm and a gate leakage current (I_{GS}) on the order of 10^{-10} A/mm. Small-signal measurements show a current-gain cutoff frequency (f_T) of 71.5 GHz and a maximum oscillation frequency (f_{MAX}) of 173.1 GHz under enhancement-mode operation. In addition, robust large-signal performance is achieved at 28 and 38 GHz, together with low noise figures across 24–45 GHz. These results establish the proposed recess-free GaN-on-Si HEMT as a scalable and RFIC-ready device platform for millimeter-wave front-end applications.

Tu3A-2 13:50
GH10-10 Nonlinear Thermal Model Capability & 3W SatCom HPA

Samira Bouzid-Driad[1], Frederic Drillet[1], Christophe Chang[1], Manfred Madel[2], Kimon Vivien[1], Laurent Brunel[1], Romain Pecheux[1], Herve Blanck[2], Valeria Di Giacomo-Brunel[1]; [1]UMS, France, [2]UMS, Germany

Abstract: This paper presents a comprehensive study of the thermal behavior of a 0.1-µm GaN HEMTs technology. An accurate electro thermal model is developed as an intermediate interface between the HEMT device process and MMIC design. The proposed model accurately predicts device characteristics over a wide temperature range. The model is validated at both the transistor level and through MMIC high power amplifiers operating up to the V-band.

Tu3A-3 14:10

Fully Aluminum-Based 0.25μm 20V GaN-on-Si Process with 3W/mm for FR3

Hsien Shun Wu, Yuan Gao, Qingyun Xie, Yi Heng Leong, Wee Leng Ong, Lakshmi Kanta Bera, Navab Singh, Geok Ing Ng; A*STAR, Singapore

Abstract: This paper reports a fully aluminum (Al)-based 0.25 μm GaN-on-Si HEMT process for FR3 application. HEMT transistor was designed in D-mode based on AlGaN/GaN structure equipped with an AlN spacer and a C-doped buffer on an 8-inch high-resistivity silicon wafer. The on-wafer characterizations with the prototyping wafer fabricated show a current collapse (CC) less than 7.5% under gate and drain stress. With a drain voltage of 20 V, the RF power density under 3 dB gain compression at 3.5 and 7 GHz are 3.4 and 3.1 W/mm, respectively. The linearity tests at same two center frequencies with 50 MHz two-tone spacing show the output third-order intercept point (OIP3) are 31 and 34.8 dBm.

Tu3A-4 14:30

A 4W Heterogeneous Power Amplifier with GaN-on-Si Dielets in Single-Crystal Diamond Interposer for 6G FR3 Applications

Pradyot Yadav[1], Xingchen Li[2], Danish A. Baig[2], Ruonan Han[1], Madhavan Swaminathan[3], Tomás Palacios[1]; [1]MIT, USA, [2]Georgia Tech, USA, [3]Penn State, USA

Abstract: This paper presents the design and fabrication of a heterogeneous power amplifier (PA) incorporating gallium nitride (GaN) high electron mobility transistor (HEMT) dielets into a single-crystal diamond interposer platform. 12×100 μm GlobalFoundries 130RF GaN high electron mobility transistors (HEMT) are singulated using femtosecond laser to a size of 274 μm × 400 μm for the fabrication of single transistor dielets. The diamond interposer is able to provide heat spreading, packaging and circuit build up for the dielet. The interposer features 2 redistribution layers (RDL) for metallization fabrication. The effects of the interposer on dielet load pull performance are analyzed. At 10 GHz, a 1.8 dB increase in output power (P_{out}), 1.5% increase in maximum power added efficiency (PAE), and a 0.3 dB increase in gain is observed. These insights guide the design of a power amplifier (PA) for 6G FR3 applications with a 3 dB bandwidth (BW) of 6.8–10.3 GHz that is able to provide up to 4 W of output power. From 8–10 GHz, the PA has a PAE ranging from 39.2–49.1% with respectable performance at 6 dB back off.

Tuesday 9 June 2026
13:30–15:10
Room 254AB
Session Tu3B:
Next-Generation CMOS Oscillators for RF and mm-Wave

Chair: Andrea Bevilacqua, Università di Padova, Italy
Co-Chair: Kimia T. Ansari, Danger Devices, USA

Tu3B-1 13:30

A Transformer-Based Inverse-Class-F-Like VCO with a Digitally Controlled Common-Mode Impedance Tuner

Hyunjoon Kim, Donghyeon Seong, Seungwoo Shim, Sanggeun Jeon; Korea University, Korea

Abstract: This paper presents a transformer-based voltage-controlled oscillator (VCO) with a digitally controlled common-mode impedance tuner that adjusts the second-harmonic voltage phase. A transformer-coupled LC tank exhibits dual resonances at the fundamental frequency and the second harmonic, producing an inverse-Class-F-like voltage waveform. The proposed tuner operates on a common-mode path that is largely decoupled from the differential oscillation mode, enabling second-harmonic phase tuning with limited impact on the oscillation frequency. By tuning the second-harmonic phase, the time-domain noise-to-phase conversion is reshaped, providing an additional degree of freedom for phase-noise optimization. Fabricated in a 28-nm CMOS process, the VCO achieves a phase noise of -113.9 to -112.5 dBc/Hz at 1-MHz offset across an 11.7–13.9-GHz tuning range while consuming 13.3–14 mW of dc power. The measured peak FoM and FoM_T at 1-MHz offset are 184.2 and 188.1 dBc/Hz, respectively.

Tu3B-2 13:50

A 5.56–9.09GHz Octa-Core Dual-Mode DCO Based on Multi-Tap Three-Turn Inductor Achieving 195.7dBc/Hz FoM and Wideband Flicker PN Suppression

Jiexi Weng[1], Liangqi Dong[1], Yuhao Yang[1], Guanjun Liu[1], Liheng Lou[1], Robert Bogdan Staszewski[2], Yizhe Hu[1]; [1]USTC, China, [2]University College Dublin, Ireland

Abstract: This paper presents a 5.56–9.09 GHz octa-core dual-mode digitally controlled oscillator (DCO) based on a multi-tap three-turn inductor. Owing to a frequency-independent passive gain of up to 3 and the resulting narrower conduction angle, it achieves a calibration-free wideband suppression of both thermal and flicker phase noise (PN). Fabricated in 22-nm CMOS, the DCO achieves a PN of -150.2 to -145.3 dBc/Hz and a figure-of-merit (FoM) of 195.7 to 192.5 dBc/Hz at a 10-MHz offset across a 48% tuning range. The flicker PN corner ranges from 100 to 290 kHz.

Tu3B-3 14:10

A 7.0-to-8.6 GHz Balanced Class-F^{-1} VCO with a Trifilar Transformer-Based Tank Achieving 194.5dBc/Hz FoM

Yunbo Huang[1], Zunsong Yang[1], Kai Cheng[1], Hongyu Ren[1], Xiaoyu Shan[1], Li Wang[1], Yong Chen[2], Bo Li[1]; [1]CAS, China, [2]Tsinghua University, China

Abstract: This paper presents a low phase noise (PN) balanced inverse-class-F (class-F^{-1}) voltage-controlled oscillator (VCO). The proposed trifilar transformer integrates dual symmetrical class-F^{-1} VCO cores without extra tank area, enabling balanced differential outputs. A harmonic shaping strategy featuring a strong second harmonic and a weak third harmonic is adopted to ensure an optimal figure of merit (FoM). Fabricated in a 65-nm CMOS process, the prototype VCO demonstrates a frequency tuning range from 7.0 GHz to 8.6 GHz with a state-of-the-art FoM of 194.5 dBc/Hz at 10MHz offset.

Tu3B-4 14:30

Harmonically Coupled Current-Sharing 4-Phase and 6-Phase Oscillators in 65-nm CMOS

Bahram Jafari[1], Samad Sheikhaei[2], Sankaran Aniruddhan[3], Shahriar Mirabbasi[1], Sudip Shekhar[1]; [1]University of British Columbia, Canada, [2]University of Tehran, Iran, [3]IIT Madras, India

Abstract: A technique is introduced for generating four or more multiphase signals by coupling Class-B cores through a shared tail current source. This approach eliminates additional coupling devices while enabling 2nd-harmonic coupling and current shaping to operate between Class-B and Class-C to improve phase noise. Prototypes of two-core and three-core oscillators, generating 4 and 6 phases respectively, are implemented in 65-nm CMOS. The 4-phase 5-GHz design consumes 1.2–1.33 mW and achieves a tuning range of 22% with a phase noise of -142 dBc/Hz at 10 MHz offset. The 6-phase 9.5-GHz oscillator with 17.5% tuning range achieves a phase noise of -141.6 dBc/Hz at 10 MHz offset. Both designs operate in a reliable voltage and swing regime.

Tu3B-5 14:50

A 10.66-to-15.03GHz Dual-Core Dual-Mode Series Resonance VCO Achieving 209dBc/Hz FoM_{TA}

Yichen Liu, Zhenbo Rao, Yan Wang; Tsinghua University, China

Abstract: This paper presents a dual-core dual-mode series-resonance (SR) CMOS voltage-control-oscillator (VCO). By integrating the multi-mode technique with the SR-VCO, this work achieves ultra-low phase noise while maintaining a wide frequency tuning range. A magnetic mode selection switch is implemented to better suppress mode ambiguity. Fabricated in a 65 nm CMOS process, the presented VCO achieves a 34% tuning range and a phase noise of -140 dBc/Hz at 10 MHz offset across the entire frequency range, with a corresponding FoM_{TA} of 209 dBc/Hz.

Tuesday 9 June 2026
13:30–15:10
Room 257AB
Session Tu3C: Advanced Integration Technologies for Power Amplifier and Low-Noise Amplifier Design

Chair: Alexandre Giry, CEA-Leti, France

Co-Chair: Gernot Hueber, United Micro Technology, Austria

Tu3C-1 13:30

3D-RDL and Bondwire Technology Comparison for Implementation of a 10W Broadband Three-Way LDMOS Doherty Power Amplifier

Mohadig Rousstia[1], Ayad Ghannam[2], Mariano Ercoli[3], John Gajadharsing[1]; [1]Ampleon, The Netherlands, [2]3DiS Technologies, France, [3]Ampleon, France

Abstract: This paper presents a novel 3D-redistribution layer (3D-RDL) passive technology for a high-efficient broadband Doherty power amplifier (DPA). The comparison with the DPA reference based on bondwire technology is provided. The realized DPA in both technologies is based on the same integrated three-way Doherty LDMOS die and is assembled in land-grid array (LGA) package. The measured S-parameter, large-signal gain and efficiency are compared. Moreover, the linearized efficiency and adjacent channel power ratio (ACPR) will be reported for different output back-off (OBO). It will be shown through measurement that with 3D-RDL Doherty combiner, the efficiency dispersion at 8dB OBO is reduced by 3%-point over the band of 3.4–3.8 GHz, and the linearized ACPR with instantaneous bandwidth (IBW) of both 300 and 400 MHz is improved by 2.5 dB. With 41dBm saturated power, this miniaturized 4.5×4 mm^2 LGA DPA is suitable for mMIMO base-station driver and small-cell applications.

Tu3C-2 13:50

A 10-W 7-GHz GaN-on-Si Doherty Power Amplifier with Hybrid MMIC-Module Integration for 6G Base-Station Applications

Kyung Pil Jung, Seunghoon Jee, Seung Hun Kim, Sungjae Oh, Jungsik Kim, Dongki Kim, Seong-Kyun Kim; Samsung, Korea

Abstract: This paper presents a 7-GHz GaN-on-Si HEMT Doherty power amplifier (DPA) with a fully integrated on-chip Doherty combiner. The hybrid MMIC-module architecture ensures precise Doherty operation with enhanced bandwidth, while maintaining the flexibility of board-level matching networks. The DPA MMIC occupies a compact core area of 1.17×2.25 mm^2. The measured DPA evaluation board (EVB) achieves a peak gain of 8 dB and a saturated power (P_{sat}) of 41.3 dBm at 7.4 GHz. For the 64-QAM 100-MHz OFDM signals, the DPA provides an average output power (P_{avg}) of 32.7–33.8 dBm, resulting in a drain efficiency (DE) ranges of 39–43.9% at P_{avg}, while an adjacent channel leakage ratio (ACLR) satisfies below -28.5 dBc at P_{avg} across carrier frequencies from 7 to 8 GHz. To the best of the authors' knowledge, this study represents the first implementation of a partially integrated MMIC Doherty architecture using GaN-on-Si process at 7 GHz.

Tu3C-3 14:10

A 60GHz LNA and PA Achieving 5dB NF and 35.6% Peak PAE in a Gate-All-Around (GAA) CMOS Process with Backside Power Delivery

Steven Callender[1], Ibukun Momson[1], Awani Khodkumbhe[2], Ali Niknejad[2], Said Rami[1], Stefano Pellerano[1]; [1]Intel, USA, [2]University of California, Berkeley, USA

Abstract: This paper presents prototype designs for a 60GHz LNA and PA in a leading-edge logic process node featuring gate-all-around (GAA) CMOS transistors and backside power delivery (BSPD). Layout optimization for the amplifier unit cell (NDP) is described. Impact of magnetic feedback within the NDP array is also discussed and a mitigation technique is presented. The fabricated LNA achieves a peak gain of 27.3dB and minimum NF of 5dB while consuming 12.6mW. The PA achieves a peak gain of 22.8dB at 55GHz. At 57.5GHz, P_{sat}/OP_{1dB}/Peak PAE are 13.5dBm/8.5dBm/35.6% under a 0.9V supply and 14.7dBm/10.8dBm/35.7% under a 1V supply.

Tu3C-4 14:30

A Wideband and Linear 300GHz Power Amplifier in 130nm SiGe BiCMOS Technology

Enrico Jimenez Tuero, Seyyid Dilek, Andrea Malignaggi, Corrado Carta; IHP, Germany

Abstract: This article presents an integrated power amplifier operating in the WR3.4 waveguide band between 220 and 325 GHz. The circuit is implemented in an 130nm BiCMOS technology, which offers heterojunction bipolar transistors with f_t/f_{max} of 500/610 GHz. Measurements show a peak gain of 21 dB, an output-referred 1 dB compression point of 11.9 dB and a saturated output power of 13.2 dBm, resulting in a peak power-added-efficiency of 4.7%. The 3 dB bandwidth reaches 96 GHz in large signal operation. The amplifier occupies an extremely compact core area of 280 μm × 150 μm. To the best knowledge of the authors the circuit showcases the highest saturated output power and 1dB compression point among the single core SiGe power amplifiers operating above 200 GHz.

Tuesday 9 June 2026
15:40–17:20
Room 252AB
Session Tu4A:
Energy-Aware RF Techniques for Sensing and Communication
Chair: Hamidreza Aghasi, University of California, Irvine, USA
Co-Chair: Chen Jiang, Fudan University, China

Tu4A-1 15:40
A 533μW Fast Duty-Cycled Pulsed-LO Beam-Steering Receiver
Yasir Al-Theyabi, David D. Wentzloff; University of Michigan, USA

Abstract: This work presents a mixer-first zero-IF pulsed-LO beam-steering receiver operating at 2.4 GHz. The receiver leverages a pulsed LO delay-locked to an external reference (XO). The delay-chain and pulse-combining architecture settles quickly and eliminates the need for PLL, thereby saving power while maintaining phase coherence. Beam steering is implemented entirely in the LO domain through quadrature LO rotation and fine delay tuning. Receiver power and performance scale with the pulsed-LO duty-cycle (D_0), controlled by XO frequency, enabling a single-knob power-performance trade-off. At a D_0 of 93.5%, the receiver consumes 533 μW and achieves an EVM of -33.4 dB, while at 11.4% it reduces to 65 μW with an EVM of -18.1 dB. The chip is implemented in 65-nm CMOS and measured in an anechoic chamber with an array of patch antennas. The receiver achieves a per-element noise figure of 13 dB and a phase resolution of 9°.

Tu4A-2 16:00
MSCR: Multi-Source-Collaborative Reconfigurable RF Energy Harvester with 3-D MPPT Achieving -32dBm Sensitivity and 8× Boost in Available Output Power
Yunzhi Ma, Yiming Liu, Haoyu Chen, Yongling Zhang, Lei Qiu, Miao Meng; Tongji University, China

Abstract: This paper presents a multi-source-collaborative reconfigurable RF energy harvesting (MSCR-RFEH) interface IC that can efficiently harvest and combine the energy from four RF sources. The proposed interface can regulate three loads at different voltages using a single-input multiple-output (SIMO) buck-boost dc-dc converter with low cascading loss. It implements a novel event-triggered 3-D maximum power point tracking (MPPT) achieving self-adaptive regulation and high MPPT accuracy by optimizing the rectifier reference voltage, searching the rectifier effective stage and regulating the converter input. Fabricated in a 65 nm CMOS process, the proposed interface IC achieves 32.2% peak efficiency, -32 dBm sensitivity, 99.2% peak MPPT accuracy, and a 10.5 dB input range with efficiency >20%. Compared to the single-source reconfigurable architecture, it achieves a 6 dB improvement in sensitivity and an 8× boost in available output power.

Tu4A-3 16:20

High Resolution Active True Time Delay with Quasi-Quadrature Generator with 31.7dB/ 500MHz Self-Interference Cancellation for Full-Duplex Communication

Eunji Jeong[1], Eunchae Jo[1], Honghyun Jeon[1], Haram Park[1], Hyeonwon Song[1], Taehyeon Kim[1], Subin Lim[1], Seong-Mo Moon[2], Seunghyun Jang[2], Seunguk Oh[3], Taehwan Jang[3], Seungchan Lee[1], Songcheol Hong[4], Jinseok Park[5]; [1]Chonnam National University, Korea, [2]ETRI, Korea, [3]Hanyang University, Korea, [4]KAIST, Korea, [5]UNIST, Korea

Abstract: A high resolution active true time delay (ATTD) with quasi-quadrature (QQ) generator for RF self-interference cancellation (SIC) for full-duplex (FD) system is presented. Unlike conventional RF SICs based on phase shifter (PS) that exhibits narrowband characteristics due to phase control, the proposed ATTD enables wideband SIC by finely controlling the time delay. A QQ generator produces two signals with a relative time-delay difference. By adjusting the ratio of the two signals, this approach can finely controls both the time delay and gain. The proposed ATTD was designed for 7.1–8.5 GHz operation and fabricated in a 65-nm bulk CMOS process with a core area of 1.77 mm^2. The design provides a fine 0.25-psec delay and 0.2 dB gain control resolution, enabling high and wideband SIC. In modulated-signal measurements, the ATTD achieves 31.7 dB SIC over 500 MHz bandwidth at 8.5 GHz while consuming only 7 mW of DC power.

Tu4A-4 16:40

A 1×2cm Localization Tag with a 2.92GHz Transmitter Chipset for LEO Satellite Localization Using Hardware and Algorithm Co-Design

Yunfan Wang[1], Rahul Narasimha[1], Steve Young[1], Yi Shen[1], Zhen Feng[1], Demba Komma[1], Seokhyeon Jeong[1], Qirui Zhang[1], Andrea Bejarano-Carbo[1], Jiajun Tang[1], Chien-Wei Tseng[1], Guanchen Tao[1], Yufan Yue[1], Taekwang Jang[2], Hun-Seok Kim[1], David Blaauw[1]; [1]University of Michigan, USA, [2]ETH Zürich, Switzerland

Abstract: This paper presents a miniature localization tag for LEO satellite localization using algorithm-hardware co-design. On the algorithm side, we achieve 10 dB reduction in required EIRP while maintaining localization accuracy. On the hardware side, we demonstrate the smallest form factor and a complete integrated Tx system including a 1×1 cm antenna and a 0.95 cm-diameter battery.

Tuesday 9 June 2026
15:40–17:20
Room 254AB
Session Tu4B: mm-Wave Front-End Building Blocks for Signal Amplification and Generation

Chair: Marco Vigilante, Qualcomm, USA

Co-Chair: Sensen Li, University of Texas at Austin, USA

Tu4B-1 15:40

Design and Comparison of Two SiGe Complementary Millimeter-Wave Power Amplifiers

Wei Ma, Weiqing Wang, Fangkai Wang, Hanzhong Xu, Xudong Wang; Nankai University, China

Abstract: This paper focuses on two complementary stacked bipolar power amplifiers (PAs): two-transistor stack and four-transistor stack. Based on the advanced 130-nm SiGe BiCMOS process, a comprehensive comparison is carried out regarding complementary mechanism, circuit topology, key performance parameters and parasitic effects. Through systematic formula derivation and analysis, their performance boundaries and design trade-offs are revealed. The measurement results show that the two-transistor stack achieves superior power-added-efficiency (PAE) of 25% with 20.5-dB gain and 17-dBm saturated output power at 24 GHz. Higher output power of 20 dBm and more competitive gain of 25 dB are obtained by the four-transistor stacked PA with 21.7% PAE. Both of the two designs exhibit excellent overall performance, demonstrating an optimal balance among gain, efficiency, and output power. Furthermore, a compact area of approximately 0.08 mm^2 is achieved by eliminating the need for power-combining and choke inductors. It is promising for area-constrained high-performance bipolar millimeter-wave power amplifier designs.

Tu4B-2 16:00

A Millimeter-Wave Frequency Reconfigurable Dual-Band T/R Front-End for 2.5:1 VSWR-Resilient in Tx Operation

Zikang Hu, Yanchen Lin, Wen Rao, Li Gao, Xiu Yin Zhang; SCUT, China

Abstract: This paper presents a frequency reconfigurable dual-band load-insensitive transmit/receive (T/R) front-end (FE). The proposed T/R FE chip is composed of a frequency reconfigurable dual-band load-insensitive power amplifier (PA), a frequency reconfigurable dual-band low-noise amplifier (LNA), and a compact ultra-wideband T/R switch at the antenna interface. Frequency reconfigurability is realized by integrating switches into matching networks. TX load insensitivity is realized by balanced architecture and a novel proposed cross-coupled adaptive bias scheme. Fabricated in 28-nm bulk CMOS process, the measured results show that in RX mode, the FE realized a peak gain of 15.2/18.2 dB at low band and high band with bandwidths of 21.5–27 GHz and 28.5–37.5 GHz, respectively. The NF at both bands is smaller than 5.5 dB. In TX mode, the FE realized a peak gain of 21.1/20.4 dB at low band and high band with bandwidths of 22.8–29.5 GHz and 30–36.8 GHz, respectively. The OP1dB/Psat/PAEmax are larger than 15.8 dBm/16.6 dBm/11.8% at both

bands. Under load variations corresponding to a voltage standing-wave ratio (VSWR) of 2.5:1, the proposed FE exhibits gain/OP1dB deviations from the 50-Ω condition of less than 1.7/2 dB at the low band, and less than 1.5/1.7 dB at the high band, respectively. To the best of the authors' knowledge, this is the first front-end that achieves band switching with TX VSWR-resilient performance.

Tu4B-3 16:20

A 47-to-100GHz Oscillator-Embedded Artificial Transmission Line Based LO Generator Achieving Averaged FoMt of -193.7dBc/Hz

Wei Sun, Benyamin Fallahi Motlagh, Boxun Yan, Aydin Babakhani; University of California, Los Angeles, USA

Abstract: This paper presents an octave-bandwidth millimeter-wave local oscillator (LO) generator architecture covering a frequency range from 47 to 100 GHz. The proposed LO generator comprises six oscillator-embedded artificial transmission line (OATL) unit cells. Each OATL cell is designed to oscillate within a designated frequency sub-band when activated; collectively, the six oscillators provide continuous frequency coverage across the entire 47–100 GHz range. When an OATL unit cell is deactivated, it contributes only a parasitic capacitance to the main signal path, which is naturally absorbed into the periodic transmission-line structure without degrading the overall operation. Each oscillator employs a gm-boosted cascode Colpitts topology to enhance start-up and improve load-driving capability. And an inductor-based tuning technique is adopted to replace the conventional capacitor-based tuning approach. The chip is fabricated in a 65-nm CMOS process and achieves a continuous frequency tuning range from 47 to 100 GHz, corresponding to a 72.1% tuning range. The measured DC power consumption varies from 9.6 to 27.6 mW across the tuning range, providing -6.5dBm to -2dBm output power at a single output. The measured phase noise at a 10 MHz offset for the six sub-band VCOs is -116, -114, -118, -117, -114, and -112 dBc/Hz, respectively. This work achieves an averaged FoMt of -193.7 dBc/Hz and the best case FoMt of -199.8 dBc/Hz.

Tu4B-4 16:40

A Blocker-Tolerant K-Band LNA with 52-dB Ka-Band TX Rejection for Satellite Communications

Heyi Sun, Chenxi Zhao, Yiming Yu, Huihua Liu, Yunqiu Wu, Kai Kang; UESTC, China

Abstract: This paper presents a blocker-tolerant K-band low-noise amplifier (LNA) in a 55-nm SOI CMOS process. A gain-flattening notch amplification unit is proposed to simultaneously enhance interference immunity and improve in-band gain flatness by exploiting parasitic effects. Furthermore, a hybrid passive filtering technique is introduced to realize comprehensive suppression of Ka-band transmitter (TX) leakage. Measurement results demonstrate a 3-dB bandwidth of 16.8–21.7 GHz with a peak gain of 29.5 dB and a minimum noise figure (NF) of 1.7 dB. Notably, an out-of-band (OOB) rejection of >52 dB is achieved. Drawing 10 mA from a 2.4-V supply, the LNA exhibits an in-band input 1-dB compression point (IP_{1dB}) of better than -30 dBm, while the blocker IP_{1dB} in the TX band (27.5–31 GHz) exceeds 0 dBm. The demonstrated superior blocker resilience makes the design highly suitable for compact multi-channel phased-array receivers in satellite communications.

Tu4B-5 17:00

A General-Purpose Schematic-Layout Co-Optimization Platform for RFIC Design Demonstrated with a 1.7-dB-NF 12–28GHz LNA

Yuwen Tao[1], Xiangyu Meng[1], Pengfei Bai[1], Junbin Ouyang[1], Baoyong Chi[2]; [1]Sun Yat-sen University, China, [2]Tsinghua University, China

Abstract: To address electromagnetic circuit interaction challenges in passive networks of RF/mm-wave integrated circuits (ICs), this paper proposes a fully automated schematic-layout co-optimization framework. Its key innovations include parametric layout generation for arbitrary passive structures and concurrent tuning of both schematic and layout parameters based on a Bayesian optimization core. The framework is validated by fabricating a 12–28 GHz low-noise amplifier (LNA) with a multi-group coupled transformer in a 65-nm CMOS process. Measurement results show that the LNA achieves 17.1dB gain, 1.7–3 dB noise figure (NF), and -15.8dBm IP1dB. As the first fabrication-verified automated co-optimization solution for full-band RFICs, this work significantly shortens the design cycle while ensuring performance robustness.

Tuesday 9 June 2026
15:40–17:20
Room 257AB
Session Tu4C: Advances in Devices and Circuits for System Integration
Chair: Matilda Livadaru, RTX, USA
Co-Chair: Florian Voineau, STMicroelectronics, France

Tu4C-1 15:40
Accurate, High Coverage On-Chip Built-In Self-Test Adopting Precision-Enhanced Power Detection and Multipath Loopback for mmWave Radar IC Measurements
Doyoon Kim, Kyunghwan Kim, Geonho Park, Goeun Baek, Byeong-Taek Moon, Hyun-Chul Park, Chan-Hong Park; Samsung, Korea
Abstract: Testing of millimeter-wave integrated circuits become increasingly challenging as operating frequencies and channel counts continue to scale, leading to high test cost and long measurement time. This paper presents an on-chip built-in self-test (BIST) architecture that enables various testing with high accuracy using internal loopback paths, compact directional couplers, and distributed power detectors. To achieve accurate power sensing within a limited area, a novel directional coupler is proposed, achieving enhanced directivity to fully separate the induced and reflected signal. The proposed BIST architecture is fabricated in a 28-nm CMOS technology. Measurements have been done with BIST, obtaining less than 1 dB measurement error in key RF and IF parameters. The proposed BIST architecture has acquired 82% of internal test coverage.

Tu4C-2 16:00
Dual-Mode Circular Cavity Filters via Azimuthal Wave Propagation
Mustafa Bakr[1], Smain Amari[1], Uwe Rosenberg[2]; [1]University of Oxford, UK, [2]Mician Global Engineering, Germany
Abstract: Dual-mode circular cavity filters are conventionally analyzed by coupling between degenerate resonances. We develop an alternative formulation based on electromagnetic waves propagating in the azimuthal direction. The dispersion relation, derived from the radial boundary condition on Bessel functions, determines a frequency-dependent propagation constant that enters the transmission matrix of each angular section. Transmission zeros arise when counter-propagating waves traversing two parallel paths cancel at the output port. This formulation encodes dispersion, characteristic impedance, and electrical length in a unified transmission-matrix framework, enabling direct synthesis from the cavity geometry. Measured results for a 6.74 GHz dual-mode filter with two transmission zeros confirm the predicted response.

Tu4C-3 16:20

Sub-60fs RFSOI Switch Performances in Advanced 200mm 130/65nm Hybrid Technology

Robin Bousmaha-Jouve[1], Julien Dura[1], Julien Amouroux[1], Pascal Masson[2], Remy Vauche[3], Frederic Gianesello[1], Wenceslas Rahajandraibe[3], Julien Babic[1], Romain Laire[1], Fayrouz Haddad[3], Pascal Fornara[1], Franck Julien[1], Clement Charbuillet[1], Alain Fleury[1]; [1]STMicroelectronics, France, [2]Polytech'Lab (EA 7498), France, [3]IM2NP (UMR 7334), France

Abstract: RF Front End Modules (FEMs) are currently achieved using a variety of technologies. However, integration has driven the wireless business to achieve appropriate cost and form factor, and CMOS Silicon-on-Insulator (SOI) was adopted about 10 years ago and is now the dominant technology for Radio Frequency Switches (RF SW) in RF FEMs for cell phones and Wi-Fi [1]. While RF SW performances integrated on RF SOI technologies have exceeded what was feasible using GaAs technologies, 6G systems require even more stringent performances and consequently RF SOI technologies must continue to be improved. In this paper, the optimization of an advanced 200 mm RF SOI technology, which achieves a record $R_{ON} \times C_{OFF}$ of 60 fs by introducing 65 nm gate length at the Front End of the Line (FEOL) to reduce the channel resistance, is proposed and discussed. Furthermore, an innovative air gap process option at the Back End of the Line (BEOL) is proposed to achieve parasitic capacitance reduction.

Tu4C-4 16:40

A 9–11GHz Multistage Switched-Capacitor Delay Element and Signal Repeater Achieving 4.6–71.4ns Delay and 40dB Gain

Travis Forbes, Benjamin Magstadt, Robert Costanzo, Jesse Moody; Sandia National Laboratories, USA

Abstract: A 9–11 GHz delay element and signal repeater device employing a passive multistage switched-capacitor approach operating in the alias regime is presented. The proposed approach enables tens of ns of delay at X band frequency while limiting the required sample rate and power consumption. On-chip chopping operation further enables larger gains for signal repeating applications. The device was implemented in a 45 nm SOI CMOS process and achieves a 4.6–71.4 ns programmable delay range with 125 ps resolution across a 3-dB bandwidth of 2 GHz. The device achieves 40 dB maximum gain, 3.8 dB minimum noise figure, and consumes 123 mW from a 1V supply with an active area of 0.75 mm^2.

Tuesday 9 June 2026
15:40–17:20
Room 255
Session Tu4J: Transceiver Architectures for Ultra-Low Power IoT

Chair: Pierluigi Nuzzo, University of California, Berkeley, USA
Co-Chair: Yao-Hong Liu, imec, The Netherlands

Tu4J-1 15:40

A 2.4GHz 369-μW Low-Latency WuRX with Voltage-to-Frequency Digital Demodulation and Bit-Error Correction

Hui Zhang, Dong Liang, Linhao Ma, Zongle Ma, Qing Li, Keping Wang; Tianjin University, China

Abstract: This paper presents a 2.4GHz wake-up receiver (WuRX) featuring low wake-up latency, high energy efficiency, and bit-error-correction capability. The design employs a novel voltage-to-frequency conversion high-energy-efficiency digital demodulation architecture and integrates a digital correlator with bit-error correction capability to enhance communication security. Fabricated in 40nm CMOS technology, the WuRX prototype achieves a wake-up latency of 19.6μs and an energy efficiency of 590pJ/b at a data rate of 625kbps, with a sensitivity of -67.6dBm and a power consumption of 369μW.

Tu4J-2 16:00

A Battery-Less Crystal-Less Event-Driven UWB Tag with Hybrid Power Management Network and PI-CDR-Based Wake-Up Receiver

Bowen Wang, Rong Zhou, Jianhang Yang, Xianlong Xiong, Minsong Zhang, Nannan Shi, Xin An, Zhangming Zhu; Xidian University, China

Abstract: Ultra-wideband (UWB) tags are widely used in inventory-management and location-tracking applications, where low-power and cost-effective connectivity are essential. In this work, we propose a battery-less and crystal-less UWB tag, composed of an ultra-low-power (ULP) wake-up receiver (WuRX) and an edge-combining all-digital UWB transmitter. The UWB tag employs a fully event-driven architecture, significantly reducing standby power consumption. Additionally, a fast-response phase-interpolation clock-and-data recovery (PI-CDR) circuit is integrated into the WuRX, which not only replaces the off-chip crystal oscillator but also tracks clock drift from the base station. Furthermore, the edge-combining all-digital UWB transmitter does not require a phase-locked loop (PLL) or an open-loop oscillator, enabling a fast startup time and low-power transmission. Implemented in 65nm CMOS, the proposed UWB tag achieves an energy harvesting (EH) sensitivity of -29dBm with receiver active and standby power consumptions of 98nW and 8nW, respectively.

Tu4J-3 16:20

An 802.11b-WiFi Backscatter Modulator Featuring 30dB PSLR with All-Digital Gaussian Pulse Shaping

Yongling Zhang, Miao Meng; Tongji University, China

Abstract: This paper presents a spectral- and energy-efficient backscatter tag that generates 802.11b-WiFi packets that can be directly decoded by WiFi access points (APs). This is accomplished by: 1) proposing a pulse-shaped, frequency-translating BPSK backscatter modulator utilizing an all-digital Gaussian filter; and 2) implementing a low-voltage phase-locked loop (LVPLL) and an on-chip WiFi Barker processor to transform an RF tone into directly decodable backscattering WiFi packets. The proposed pulse-shaped modulator achieves a peak sidelobe ratio (PSLR) of 30 dB, representing a 17 dB improvement over conventional BPSK backscatter modulators, and an error vector magnitude (EVM) of 13.2%–15.5% at 11 Mb/s, all while consuming 19 μW. Wireless over-the-air measurements demonstrate a worst-case TX-to-Tag-to-RX range (with equal TX-to-Tag and Tag-to-RX distances) of 40 m for the pulse-shaped 802.11b-WiFi uplink when excited by a 30 dBm EIRP tone generator.

Tu4J-4 16:40

A Fully Integrated 2.4GHz BLE Transmitter with ADPLL and Class-G Switched-Capacitor PA Achieving 30% System Efficiency

Chen-Hsing Hsu[1], Yi-Chen Hsiao[1], Yu-Che Yang[2], Sheng-Chiang Tu[2], Yi-Chang Shih[2], Ka-Un Chan[2], Yu-Te Liao[1]; [1]NYCU, Taiwan, [2]Realtek Semiconductor, Taiwan

Abstract: This work proposes a 2.4-GHz Bluetooth Low-Energy (BLE) transmitter that delivers high output power with high system efficiency. The chip is fabricated in a 40-nm CMOS process and occupies a chip area of 0.56 mm^2, integrating a divider-less all-digital phase-locked loop, featuring a Class-C digitally controlled oscillator and a DTC-assisted TDC, and a single-ended Class-G switched-capacitor power amplifier with enhanced coding to improve power back-off efficiency across a wide output range. The transmitter supports -26.8 dBm to +8.15 dBm output power and achieves 30.39% peak system efficiency at +8.15 dBm while satisfying BLE emission mask requirements.

WORKSHOPS

Workshops are offered on Sunday, Monday and Friday at the Thomas M. Menino Convention & Exhibition Center (MCEC). Please see daily handout on Sunday, Monday, and Friday in the registration area and from volunteers throughout the meeting floors to confirm room location.

WSA (Full-Day): Sunday 08:00–17:20
Advanced RF to Sub-THz Frequency Generation: Oscillators, Frequency Multipliers, and their Applications

Sponsor: **RFIC**

Organizers: **Teerachot Siriburanon**, *University College Dublin*
Jingzhi Zhang, *UESTC*
Salvatore Finocchiaro, *Qorvo*

Abstract: This workshop will present recent breakthroughs in the design of Voltage Controlled Oscillators (VCOs) and frequency multipliers, with a focus on innovations spanning the microwave, mm-wave, and sub-THz frequency bands. As these components are critical enablers in emerging communication, radar, and sensing systems, the workshop will cover both theoretical insights and practical design strategies that push the boundaries of performance, integration, and power efficiency. Bringing together leading experts from both academia and industry, the sessions will highlight state-of-the-art circuit techniques, emerging device technologies, and system-level considerations. Presentations will explore various aspects of VCO and frequency multiplier design, aiming to achieve low noise, wide tuning range, and high efficiency. The workshop will also address key challenges in scaling designs to higher frequencies and more compact integration.

Speakers:

1. "Bulk Acoustic Wave (BAW) Oscillators for Timing Reference and Frequency Generation", **Bichoy Bahr**, *Texas Instruments*
2. "mm-Wave Oscillator Design", **Jun Yin**, *University of Macau*
3. "Pushing the Boundaries of Purity: Techniques for Ultra-Low Phase Noise CMOS Oscillators", **Wei Deng**, *Tsinghua University*
4. "Designer-Inspired AI-Assisting Methods for Power-Efficient RF Oscillator Design", **Wei-Han Yu**, *University of Macau*
5. "Advanced Coupling Techniques for Low-Noise and Quadrature Oscillators", **Andrea Bevilacqua**, *Università di Padova*
6. "Low-Noise, High-Frequency VCO and Multiplier Designs for mm-Wave Radar Applications: Circuit and System Considerations", **Krishnanshu Dandu**, *Texas Instruments*
7. "Frequency Generation Toward Sub-THz: Design Considerations and Circuit Techniques", **Heein Yoon**, *UNIST*
8. "mm-Wave and Sub-THz Frequency Multiplier Chain Design: Harmonic Generation, Impedance Optimization, and Buffering Techniques", **Sehoon Park**, *Kyungpook National University*

WSB (Full-Day): Sunday 08:00–17:20
Beamforming Architectures and Circuits for Next-Generation Commercial and Defense Systems

Sponsors: **RFIC, RFSA**

Organizers: **Salvatore Finocchiaro**, *Qorvo*
Akshay Visweswaran, *Nokia Bell Labs*

Abstract: The workshop takes a deep dive into systems and circuits at the forefront of the next generation wireless technology for commercial and defense applications. Bringing together leading experts from both academia and industry, the talks will highlight trade-offs in MIMO systems that motivate the use of analog, digital and hybrid beamforming with a focus on parameters like coverage, spectral and energy efficiency, bandwidth and throughput. Emerging device technologies, state-of-the-art design techniques for RF, analog and digital circuits, advanced packaging integration and thermal management will also be presented, providing a comprehensive view of the direction in which wireless systems are heading.

Speakers:

1. "Architectures for Large-Scale Phased Arrays in 5G, 6G and SATCOM", **Harish Krishnaswamy**, *Columbia University*
2. "Unlocking the Potential of FR3 with Giga-MIMO and 6G Innovations", **Kiran Mukkavilli**, *Qualcomm*
3. "Array Design Consideration for W-Band and Beyond", **Eric Wagner**, *Northrop Grumman*
4. "Beamforming: Balancing with CMOS and III-V from Microwave to mm-Wave Frequencies", **Yang Zhang**, *imec*
5. "Reconfigurable Everything for 6G Software Defined Radios at 6–18GHz — Beamformer ICs and Up/Down-Converters", **Yingtao Zou, Haisu Ju, Gabriel M. Rebeiz**, *University of California, San Diego*
6. "Wideband, Squint-Resilient Beamforming in Ku-Band Hybrid Phased Arrays Using True-Time-Delay Architectures", **Jeff Massman**, *Analog Devices*
7. "A Fully Integrated RFIC for Very High Throughput Hybrid Beamforming Applications Including DPD", **Gaurav Menon, Ian Gresham**, *Qorvo*
8. "Techniques for Distributed and Fast Beam Synthesis in Phased Arrays", **Arun Paidimarri**, *IBM*
9. "Calibration and Measurement Methods for Phased Array Beamforming Antennas", **Joel Dunsmore, Mike Ballou**, *Keysight Technologies*

WSD (Full-Day): Sunday 08:00–17:20
Broadband and Spectrally Agile RF Front-Ends for Advanced Software-Defined Radios

Sponsors: **RFSA, RFIC**

Organizers: **Hamed Rahmani**, *New York University*
Arun Natarajan, *Yale University*

Abstract: Next-generation wireless systems Beyond-5G will place unprecedented demands on radio front-ends across all frequency ranges, from sub-6GHz (FR1) to the upper mid-band (FR3) and into mm-wave spectrum. Each band presents its own trade-offs in terms of coverage, capacity, propagation, and spectrum availability, but they share common challenges: fragmented allocations, coexistence with incumbent services, and the need for spectrally agile, energy-efficient, and highly integrated transceivers. The upper mid-band (FR3, ~6–24GHz) is a prime example. Compared to congested FR1 allocations, it offers an order of magnitude more bandwidth, while avoiding some of the severe propagation penalties of mm-wave frequencies above 28GHz. These advantages make FR3 highly attractive for wide-area enhanced broadband and low-latency applications, but also introduce stringent coexistence requirements with incumbent scientific, defense, and satellite users. The resulting emphasis on spectrum awareness and frequency agility highlights design challenges that resonate across all frequency ranges. This workshop will explore the circuit- and architecture-level innovations needed to enable broadband, reconfigurable, and spectrally agile radios. Topics include: Wideband, reconfigurable LNAs and PAs with high linearity and efficiency; Frequency-agile local oscillators and synthesizers with fast switching, low phase noise, and fine resolution; Wideband filtering and duplexing strategies using tunable, switched-capacitor, or acoustic/EM-based solutions; Digital-assisted calibration and adaptation, including ML-based techniques for resilience against PVT variations; Scalable architectures in advanced CMOS and SiGe technologies, enabling multi-band, multi-standard, and multi-antenna integration with energy efficiency. By bringing together experts from academia, industry, and government laboratories, the workshop will highlight state-of-the-art circuit techniques and cross-layer considerations — including spectrum policy, system-level trade-offs, and co-designed RF/digital intelligence — that are critical to realizing the next generation of programmable, energy-efficient, spectrally agile radios.

Speakers:

1. "Reconfigurable Everything for 6G Software-Defined Radios at 6–18GHz — Beamformer ICs and Up/Down-Converters", **Yingtao Zou, Haisu Ju, Gabriel M. Rebeiz**, *University of California, San Diego*
2. "Reflectionless Receiver for Microwave/mm-Wave Communication with Flat Carrier Aggregation Operation", **Xun Luo**, *Shenzhen University*
3. "Flexible, Linear and Low-Noise RF-DACs from FR1-to-FR3: A Solution for the Next G", **Jeffrey Walling**, *Virginia Tech*
4. "Building Spectrally Agile SDRs for FR3", **Sundeep Rangan**, *New York University*
5. "RF Sampling Receivers for Ka-Band Frequencies", **Josef Heel, Bram Nauta**, *University of Twente*
6. "Low-Noise High-Linearity Blocker-Tolerant Receivers: The Next Mile Toward FR3 6G", **Reza Nikandish, Hamed Rahmani**, *New York University*

7. "Blocker-Tolerant Mixer-First Receivers for 5G-Advanced/6G FR1/FR3 Communications", **Keping Wang**, *Tianjin University*
8. "Unleashing the THz Band: From Near-Field to Space", **Josep Jornet**, *Northeastern University*
9. "Slice-Based True-Time-Delay Receiver Arrays with Adaptive Real-Time Beam Tracking for Next-Generation Flexible Wireless Systems", **Subhanshu Gupta**, *Washington State University*

WSE (Full-Day): Sunday 08:00–17:20
Dare to Dream – The Path to True Batteryless Radios

Sponsor: **RFIC**

Organizers: **Zeshan Ahmad**, *Coherent*
Kuo-Ken Huang, *Everactive*

Abstract: Are we there yet? — a world where radios and SoCs for IoT and countless other domains are truly battery free? What would it take to go beyond a smart toaster to a future with ubiquitous ambiently powered sensors that work seamlessly with the existing wireless devices and infrastructure. This workshop addresses these questions by bringing together a unique mix of top industry, research and academic speakers with expertise ranging from RFICs to SoCs. Apart from the current state of the low-power radios, the talks will discuss circuits and system architectures that have the potential to achieve 1000× improvements in energy efficiency. The workshop and concluding panel session also aims to explore salient features which the front-ends, integrated energy harvesters, and overall systems must provide to continue the evolution of ambient IoTs.

Speakers:
1. "Brief Workshop Introduction", **Zeshan Ahmad**, *Coherent*
2. "Ambient IoT: Powering and Connecting the Next Information Frontier", **Patrick Mercier**, *University of California, San Diego*
3. "The Path Towards Ambient IoT", **Danielle Griffith**, *Texas Instruments*
4. "Wake-Up Radio Compliant with IEEE802.11ba for Scavenging Energy Sources Integrated in 18nm FD-SOI CMOS Technology", **Elio Guidetti**, *STMicroelectronics*
5. "From Sensitivity to Selectivity: Circuit Design Challenges in WuRX", **Jesse Moody**, *University of Maryland at College Park*
6. "The State of Battery-Less Radio: A System Perspective Across Diverse Wireless IoT Standards", **Kuo-Ken Huang**, *Everactive*
7. "Sub-THz Technologies Towards Ultra-Miniaturized Radio Platforms", **Ruonan Han**, *MIT*
8. "Zero-Power Smart Reflector", **Rocco Tam**, *NXP Semiconductors*
9. "Autonomous Low-Power Systems-on-Chip for in-vivo and in-vitro Biomedical Applications", **Vadim Issakov**, *Technische Universität Braunschweig*
10. "Panel Discussion", **Kuo-Ken Huang[1], Zeshan Ahmad[2]**, *[1]Everactive, [2]Coherent*

WSF (Full-Day): Sunday 08:00–17:20
Design and Implementation of FR3 Power Amplifiers

Sponsor: **RFIC**

Organizers: **Patrick Reynaert**, *KU Leuven*
Marco Vigilante, *Qualcomm*
Alexandre Giry, *CEA-Leti*

Abstract: This workshop will focus on the design and implementation of FR3 Power Amplifiers. It will cover technology considerations, circuit implementation and topology consideration for PAs in this frequency range. Both Silicon, GaAs and GaN circuit examples and techniques are discussed, as well as DPD and broadband circuit techniques. The speakers are from both academia and industry.

Speakers:

1. "Design and Implementation of FR3 Power Amplifiers for Extreme Massive MIMO", **Seongkyun Kim**, *Samsung*
2. "Design Techniques for Wideband High-Efficiency Integrated Power Amplifiers in FR1/FR3 Bands", **Ayssar Serhan**, *CEA-Leti*
3. "LMBA: Ideal Candidate for FR3 PAs?", **Roberto Quaglia**, *Cardiff University*
4. "GaAs HBTs for FR3 Power Amplifiers", **Peter Asbeck**, *University of California, San Diego*
5. "Centimeter-Wave Power Amplifiers in Silicon and III-V for 6G FR3 Applications", **Chenaho Chu**, *ETH Zürich*
6. "Advanced Supply Modulator Design for 6G FR3 RF Power Amplifiers", **Ji-Seon Paek**, *Pusan University*
7. "Advanced High Efficiency GaN PA Module for FR3 Massive MIMO Base Stations", **Shuichi Sakata**, *Mitsubishi Electric*
8. "Modeling and Compensation of Non-Linear Effects in Highly Integrated MIMO Transmit Arrays", **Christian Fager**, *Chalmers University of Technology*

WSJ (Full-Day): Sunday 08:00–17:20
Pros and Cons of Moving Above 100GHz – Circuits, Systems and Potential Applications

Sponsor: **RFIC**

Organizers: **Vadim Issakov**, *Technische Universität Braunschweig*
Sorin P. Voinigescu, *University of Toronto*

Abstract: The D-band frequency range is gaining attention for both radar and communication applications due to potential system miniaturization related to smaller wavelength and the possibility of having larger bandwidth. There is an ongoing frequency regulation activity at ETSI, ECC and FCC on standardization of new frequency bands, targeting bandwidth >10GHz. Large bandwidth is beneficial for radar to achieve good range resolution, while for communication applications one can achieve higher data-rates. Pushing operation frequencies even further beyond the D-band towards 300GHz may offer even more potentially large available unregulated bandwidth. However, these high operation frequencies reach the technological limits imposed by the available CMOS processes. Operating the transistors at frequencies beyond half of the achievable ft/fmax makes it very difficult to obtain sufficient gain and power from an amplifier stage. One possible solution would be to use III-V technologies, which offer ft/fmax frequencies by far exceeding those of advanced CMOS nodes. Still, the possibility of integrating the mm-wave front-end with the digital baseband on the same chip makes CMOS very attractive despite this mentioned drawback. Another challenge that comes at higher frequencies are the higher losses of the interconnects. The packaging possibilities. Realization of antennas (on-chip or in-package?). As well, much higher propagation losses make the link budget very challenging and make it very hard to reach ranging or communication over large distances. In this full-day workshop we will address exactly these questions: (a) does it make sense to go to frequencies above 100GHz? Or shall we stay in the comfort zone below 100GHz?; (b) for which applications does it makes sense at all?; (c) what are the circuit related challenges in silicon-based technologies and how can we solve them?; (d) what are the challenges not only to build an SoC, but to actually build a system >100GHz?; (e) discuss emerging applications that might profit by very high frequencies. Level budget considerations for various mm-wave systems will be discussed. Fair and unbiased opinions will be given by experts. The workshop features distinguished speakers from leading companies and academia, who will present their view on mm-wave circuits >100GHz, as well as sharing their "best practice" on how to design mm-wave circuits. A brief concluding discussion will round-off the workshop to summarize the key learnings on the wide range of aspects presented during the day.

Speakers:

1. "Chips and Applications Above 100GHz: Not Everything Makes Sense", **Patrick Reynaert**, *KU Leuven*
2. "3 vs. 30 vs. 300GHz: a Link Budget Analysis", **Mark Rodwell**, *University of California, Santa Barbara*
3. "System Level Considerations and Feasibility of >100GHz for Backhaul Communications", **Klas Eriksson**, *Ericsson*

4. "Wideband and Power-Efficient SiGe BiCMOS Building Blocks for D-Band Communications", **Guglielmo De Filippi[1], Andrea Mazzanti[2]**, *[1]Fondazione Chips-IT, [2]Università di Pavia*
5. "Circuit, Antenna and Package Co-Design Challenges for D-Band Radar and Communications IC", **Fabio Padovan**, *Infineon Technologies*
6. "Development of a 300GHz Band Tomographic Imaging System Using CMOS-RFIC", **Ichiro Somada, Yuki Tsukui, Akihito Hirai**, *Mitsubishi Electric*
7. "Design Considerations for mm-Wave Building Blocks Toward 300GHz in 22FDX", **Rui Zhou, Finn Stapelfeldt**, *Technische Universität Braunschweig*
8. "Phased Array Transmitter Above 200GHz", **Kenichi Okada**, *Science Tokyo*
9. "D-Band Circuits and System Design for High-Speed Wireless and Dielectric Waveguide Communications in CMOS Process", **Haikun Jia**, *Tsinghua University*
10. "Coherent Electro-Optical Transceivers for High-Speed Data Links", **Lorenzo Iotti**, *Nokia*
11. "Wideband 130–170GHz Receivers and 140GHz Dual-Pol./Dual-Beam Phased Array for 6G Systems with up to 2×50Gbps Communications", **Ahmed Afifi[1], Ahmed Quorani[2], Gabriel M. Rebeiz[2]**, *[1]NVIDIA, [2]University of California, San Diego*

WSK (Full-Day): Sunday 08:00–17:20
Taming Multi-Beam Arrays: Emerging Architectures, Algorithms, and Applications

Sponsors: **RFIC, RFSA**

Organizers: **Alberto Valdes-Garcia**, *IBM*
Emily Naviasky, *IBM*
Oren Eliezer, *Samsung*

Abstract: Scaled antenna arrays that support multiple simultaneous beams can enable significant throughput improvements and new capabilities for both communications and sensing applications. These benefits provide the form-factor and spectral efficiencies required for next generation wireless systems. However, beam scaling also scales up traditional design challenges and creates new implementation hurdles. For example, handling the signal distribution and processing for hundreds of antennas and tens of beams quickly results in stages that are power and thermally infeasible. Innovations in multi-beam array architectures are indispensable to overcoming these challenges for emerging satellite communications, radar, and 6G applications. To succeed in real-world deployments these innovations must be developed with resilience, cost-effectiveness, and hardware scalability considerations in mind. This workshop explores specifically multi-beam topics with an array of experts presenting their work on re-imagining how to architect and build point-to-multi-point arrays at scale. Approaches for beam-scaling in frequency, space, and time will be explored and hardware implementations that range from RF-centric to mostly digital will be covered. The goal is to provide attendees with an in-depth overview of this emerging area of antenna array design, and cast light on trade-offs and future directions.

Speakers:

1. "True Time Delay Array Beamforming for Initial Access, Multi-User Communications and Spectrum Sharing", **Danijela Cabric**, *University of California, Los Angeles*
2. "Multi-Layer Spatial Processing: Breaking the Complexity-Capacity Barrier in Multi-Beam Arrays", **Susnata Mondal**, *Intel*
3. "Achieving More with Less: Time-Modulated Multi-Beam Arrays for MIMO Communication and Sensing", **Hua Wang[1], Tzu-Yuan Huang[2]**, *[1]ETH Zürich, [2]ARGUS SPACE*
4. "Beamforming in a Multi-Carrier OFDM System", **Bo Göransson**, *Ericsson*
5. "Scaling to Many Beams by Choosing the Right Beamformer for the Application", **Emily Naviasky**, *IBM*
6. "InP HBT and Si CMOS mm-Wave Arrays and Links", **Mark Rodwell**, *University of California, Santa Barbara*
7. "Efficient Beamspace Processing for Large-Scale Antenna Arrays", **Zhengya Zhang**, *University of Michigan*
8. "Integrated Multi-Functional mm-Wave Arrays Based on Reconfigurable Surfaces", **Harish Krishnaswamy, Alfred Davidson**, *Columbia University*

WSL (Full-Day): Sunday 08:00–17:20
Frontiers of G-Band Innovation for Next-Generation Communication and Sensing: From Ultra-High-Speed Devices to Sub-THz Integrated Circuits and Systems

Sponsors: **RFIC, RFTT**

Organizers: **Damla Dimlioglu**, *Cornell University*
Hasan Sharifi, *HRL Laboratories*
Ahmet Çağrı Ulusoy, *KIT*

Abstract: Increasing demand for continuous information flow and uninterrupted connectivity requires next-generation communication and sensing systems to support higher data-rates and wideband operation. As a result, wireless systems are moving to higher frequencies, offering wider bandwidth and higher channel capacity, while simultaneously reducing the system size. Although lower mm-wave bands, such as V-band (40–75GHz), have been explored as a potential solution to meet the demand for high-speed connectivity, the elevated levels of atmospheric attenuation create an additional challenge for maintaining signal power in wireless transmission over long distances. On the other hand, the upper portion of the mm-wave spectrum at 110–300GHz, also known as G-band, offers a promising path to achieve higher data-rates in point-to-point links, defense applications, localization, ranging, and other multi-user communication scenarios as the underutilized portion of the EM spectrum, while enabling higher resolution in radars and other sensing systems for biomedical or security screening and also reducing the size of all these systems. The sub-THz spectrum above 200GHz is of particular interest due to lower atmospheric attenuation. However, building high-performance integrated circuits and systems at G-band poses significant disadvantages due to the lower available gain of the transistors and higher noise contribution from components, leading to higher power consumption and reduced sensitivity at

these sub-THz frequencies. Therefore, a combination of advanced circuit design techniques and system-level innovations, state-of-the-art high-speed devices harnessing the properties of compound semiconductors, heterogeneous integration, and co-design with packaging is essential to overcome the inherent challenges of the G-band design space. This workshop provides a comprehensive and in-depth review of the latest academic and industrial research on innovative techniques and cutting-edge technologies for realizing high-data-rate wireless communication and radar systems at 110–300GHz across SiGe, scaled-CMOS, InP, and GaN platforms, with particular focus on designs above 200GHz in the upper G-band. First, novel circuit techniques and topologies to enable high-power generation with maximum power efficiency, advanced high-speed device design and optimization in compound semiconductor processes, as well as III-V RF front-ends and hybrid InP/CMOS phased arrays above 200GHz, will be presented. State-of-the-art SiGe BiCMOS transceiver arrays across the entire G-band will be showcased with an emphasis on ultra-compact design and 2D scalability, along with multiple demonstrations of modular beamforming ICs supporting up to 200Gbps wireless transmission, wideband radar transceiver chips for integration in large MIMO arrays, and upper G-band MMICs enabling radar systems with multi-target resolution down to a few millimeters while maintaining an absolute ranging accuracy on the order of 1µm. In addition, system- and circuit-level design considerations for record-low-power CMOS radar sensor systems will be reviewed. Finally, co-design and co-integration of sub-THz ICs in SiGe and SOI with glass interposer technology and 3-D Heterogeneous Integrated (3DHI) phased arrays incorporating an antenna on glass, GaN-on-SiC MMICs, a silicon interposer, and a silicon Beam Forming Integrated Circuit (BFIC) will be presented as a pathway toward end-to-end communication modules in G-band for commercial and defense applications.

Speakers:

1. "Recent Progress in GaN MMICs for Wideband Applications in G-Band", **Rüdiger Quay**, *Fraunhofer IAF*
2. "Enabling High-Resolution Radars in G-Band Using SiGe MMICs", **Nils Pohl[1], Timo Jaeschke[2]**, *[1]Ruhr-Universität Bochum, [2]2π-LABS*
3. "2D-Scalable SiGe BiCMOS Front-Ends for Phased Array Communication Above 110GHz", **Dietmar Kissinger**, *Universität Ulm*
4. "G-Band Power Amplifiers Using InP HBT Technologies", **James F. Buckwalter**, *University of California, Santa Barbara*
5. "From RFICs to Systems: Realizing Sub-THz Communication Modules", **Shahriar Shahramian**, *Nokia Bell Labs*
6. "Tackling Challenges in 3-D Heterogeneous Integrated (3DHI) Phased Arrays From W-Band Through G-Band", **John Roderick**, *HRL Laboratories*
7. "High-Speed InP Front-Ends and Hybrid Phased Array Techniques for G- and J-band Future Wireless Systems", **Ibrahim Abdo[1], Hiroshi Hamada[1], Kenichi Okada[2], Hiroyuki Takahashi[1]**, *[1]NTT, [2]Science Tokyo*
8. "G-Band Signal Sources Towards Watt-Level Output Power in SiGe Technology", **Ahmet Çağrı Ulusoy**, *KIT*
9. "SiGe BiCMOS Integrated Circuits and Systems for Sub-THz Communication and Sensing", **Corrado Carta**, *IHP*
10. "Panel: Prospects of Sub-THz Integrated Circuits and Systems for Next-Generation Communication and Sensing Platforms", **Damla Dimlioglu[1], Hasan Sharifi[2], Ahmet Çağrı Ulusoy[3]**, *[1]Cornell University, [2]HRL Laboratories, [3]KIT*

WSM (Full-Day): Sunday 08:00–17:20
RFICs in Space: Design Techniques Enabling Satellite Communications and Sensing in Harsh Environments

Sponsors: **RFIC, RFSA**

Organizers: **Aly Ismail**, *Apple*
Travis Forbes, *Sandia National Laboratories*

Abstract: Emerging applications such as Low Earth Orbit (LEO) satellite-based internet and geolocation services are rapidly expanding, driven by commercial efforts to deliver low-cost satellite connectivity to consumers. However, space environments present unique challenges not encountered in terrestrial systems, including radiation-induced errors, extreme temperature fluctuations, and limited power availability. Systems operating beyond LEO face even more severe higher levels of environmental degradations. This workshop will bring together leading experts from academia and industry, spanning both LEO SATCOM and traditional space-based systems, to provide a comprehensive overview of the key design challenges and state-of-the-art techniques required for reliable RF system performance in space.

Speakers:

1. "Designing for Space: LEO, MEO and GEO Phased Arrays Using Silicon RFICs", **Gabriel M. Rebeiz**, *University of California, San Diego*
2. "Beamforming SoCs for Low-Cost, High-Capacity Space Communications", **Sherif Abdalla**, *Broadcom*
3. "Radiation Effects on Commercial All-Programmable RF-Agile Transceiver", **Jan Budroweit**, *DLR*
4. "Radiation Effects on CMOS RF/Analog Circuits and Mitigation Techniques", **Samuel Palermo**, *Texas A&M University*
5. "Developing Robust and Economical RF Solutions for Next-Generation Defense and Commercial Space Platforms", **Ryan Jennings, Winston Clarke**, *Qorvo*
6. "Phased Array Solution for SATCOM : A Modular Approach", **Shailesh Kulkarni**, *Tusk IC*
7. "Using AI to Achieve Reliability in Harsh Environments", **Amr Haggag**, *ARM*
8. "Ultra Sensitive and Wideband CMOS Radar Techniques for Moon to Mars Exploration", **Adrian Tang**, *Jet Propulsion Laboratory*

WSN (Half-Day): Sunday 08:00–11:50
Breaking Barriers in Bandwidth and Power: Advances in Distributed Amplifiers for Broadband Front-Ends

Sponsors: **RFIC, RFTT**

Organizers: **Tolga Dinc**, *Texas Instruments*
Salvatore Finocchiaro, *Qorvo*
Ying Chen, *Samsung*

Abstract: Distributed Amplifier (DA) architectures have long been valued for their ability to deliver exceptionally wide bandwidths. In recent years, new design strategies and circuit techniques in various technologies have dramatically expanded their potential in applications ranging from high-speed optical and wireless communication to defense, instrumentation, radar, and sensing. This workshop will provide a comprehensive overview of recent research and development in distributed amplifiers, focusing on performance improvements across bandwidth, output power, linearity, noise, and efficiency enhancement. Emphasis will be given to implementations across multiple technology platforms including CMOS, SiGe BiCMOS, GaN, and InP technologies, highlighting the unique opportunities and challenges in each domain.

Speakers:

1. "Bandwidth Extension, High Gain and High Isolation InP Distributed Amplifiers", **Phat T. Nguyen[1], Viet-Anh Ngo[2], Anh-Vu Pham[2]**, *[1]Keysight Technologies, [2]University of California, Davis*
2. "Broadband, Efficient mm-Wave and THz Power Amplifiers Using Advanced InP HBT Technologies", **Zach Griffith**, *Teledyne Scientific & Imaging*
3. "GaN NDPA MMIC Design for Decade Bandwidth Power and Efficiency", **Michael Roberg**, *Qorvo*
4. "Ultra-Wide Bandwidth Distributed Amplifier Topologies in CMOS RFSOI and SiGe for High Speed Wireline Applications", **Omar El-Aassar[1], Mir Mahmud[1], Hasan Al-Rubaye[2], Gabriel M. Rebeiz[3]**, *[1]Apple, [2]Lightmatter, [3]University of California, San Diego*
5. "Ultra-Wide Bandwidth Distributed Amplifiers with Applications to Optoelectronics", **Justin Kim, James F. Buckwalter**, *PseudolithIC*

WSO (Half-Day): Sunday 13:30–17:20
Advances in mm-Wave Phased Array Technologies

Sponsors: **RFSA, RFIC**

Organizers: **Nicholas Miller**, *Michigan State University*
Mauro Ettorre, *Michigan State University*
Gian Piero Gibiino, *Università di Bologna*

Abstract: Next-generation communications and sensing systems operating in the mm-wave range require a collaborative effort among the various components that make up the subsystems to enhance performance and reduce production costs. This workshop will bring together leading researchers from different fields of mm-wave phased arrays to discuss the key requirements and challenges relevant to their areas of expertise. The half-day workshop will kick off with a unique perspective on mm-wave phased arrays from industry and government representatives, providing context for the challenges and requirements in this field. The remainder of the workshop will feature internationally renowned speakers specializing in transistors, integrated circuits, packaging, and heterogeneous integration, as well as phased arrays. Interactive discussions will be prioritized throughout the event to encourage engagement among participants.

Speakers:

1. "Recent Developments and Next Generation Capabilities for Panel-Based Phased Arrays", **David Conway**, *MIT Lincoln Laboratory*
2. "InP HBT Front-Ends for High Performance mm-Wave Phased Arrays", **Adam Young**, *Teledyne Scientific & Imaging*
3. "Efficient mm-Wave Phased Array Building Blocks in Silicon Technology", **Ahmet Çağrı Ulusoy**, *KIT*
4. "Heterogeneously-Integrated T/R Chips to Enable Next-Gen mm-Wave Arrays", **James F. Buckwalter**, *PseudolithIC*
5. "Development of 10:1 Bandwidth (2.5–25GHz) Silicon Beamformers and Phased Arrays for 6G and Multi-Band SATCOM Applications", **Gabriel M. Rebeiz**, *University of California, San Diego*

WSP (Half-Day): Sunday 08:00–11:50
Next-Generation Optical Technologies Enabling Future Data Centers and Wireless Connectivity

Sponsor: **RFIC**

Organizers: **Sajjad Moazeni**, *University of Washington*
Antoine Frappé, *Université de Lille*
Bahar Jalali Farahani, *Cisco*

Abstract: The ever-increasing demand for higher network capacity, and the volume of different devices that need connectivity, require innovative solutions. In mobile applications, this demand is addressed in 5G and 6G networks by using microwave links with massive Multiple-Input Multiple-Output (MIMO) antenna arrays to support high data-rate connectivity between large number of devices with improved coverage. However, the capacity is still limited by the available RF spectrum. Radio-over-fiber (RoF) systems combined with MIMO technology offer a flexible and powerful solution for extending the reach and improving the performance of wireless networks. In data center application, the hybrid opto-electrical links presents numerous advantages over single technology solutions. Energy efficiency, higher throughput, scalability and cost can be optimized by proper convergence of the two technologies. In this workshop, experts from industry and academia will discuss the latest developments in the convergence of the opto-electrical technology as applied to mobile networks and data center connectivity.

Speakers:

1. "RF-over-Fiber: Combining Low-Loss Transportation and Photonic Processing", **Guy Torfs**, *Ghent University*
2. "Low-Power Coherent Optics to Enable Reconfigurable Networks in AI Systems", **Clint Schow**, *University of California, Santa Barbara*
3. "Package-to-Package Scale-Out Interconnect Solutions Based on In-Package Optical I/O", **Miloš Popović**, *Ayar Labs*
4. "Optical Receivers — from Coherent Transceivers to Short-Reach Scale-Up Solutions", **Mahdi Parvizi**, *Astera Labs*
5. "Coherent Silicon Micro-Ring Modulators: Unlocking Higher Bandwidth Density", **Wei Shi**, *Université Laval*

WSQ (Half-Day): Sunday 13:30–17:20
The Next Frontier in Radar Systems

Sponsors: **RFIC, RFSA**

Organizers: **Shahriar Shahramian**, *Nokia Bell Labs*
Giuseppe Gramegna, *imec*

Abstract: The frontier of next-generation radar is shaped by advances in mm-wave, UWB, and AI-assisted phased array technologies. In the D-Band, SiGe implementations enable instantaneous bandwidths up to 56GHz, delivering millimeter-level resolution and unlocking applications in imaging, non-destructive testing, and metrology. In parallel, UWB radar provides low-power, high-precision sensing for presence detection, vital-sign monitoring, and in-cabin safety. Complementing these developments, AI-driven phased arrays are emerging as enablers of adaptive beamforming, joint radar-communications (ISAC), and scalable multi-antenna architectures. This talk will highlight circuit and system design challenges, analog front-end techniques, and prototype results, illustrating how SiGe mm-wave, UWB, and AI-enhanced phased arrays together define the future of high-resolution radar.

Speakers:

1. "Charting New Frontiers in Automotive Imaging Radar Transceivers", **Kostas Doris**, *NXP Semiconductors*
2. "UWB Radar for Low-Power Applications: From Indoor to In-Cabin Sensing", **Anoop Narayan Bhat**, *imec*
3. "AI-Driven mm-Wave Phased Array Radar and ISAC", **Alberto Valdes-Garcia**, *IBM*
4. "Enabling High-Resolution Radar in the D-Band Using SiGe MMICs", **Timo Jaeschke[1], Nils Pohl[2]**, *[1]2π-LABS, [2]Ruhr-Universität Bochum*

WMI (Half-Day): Monday 08:00–11:50
Advanced Thermal Management in RF Systems: From Wide-Bandgap Materials to Industrial Implementation

Sponsors: **RFTT, RFIC, RFSA**

Organizers: **Mo Shakouri**, *Microsanj*

Abstract: The exponential demands for higher power densities, broader frequency coverage, and enhanced reliability in microwave systems have exposed fundamental limitations in conventional thermal design approaches. As next-generation applications push beyond traditional thermal boundaries — from 5G/6G infrastructure to automotive radar and space-based communications — the industry faces a critical inflection point where incremental improvements in thermal management are essential to meet performance requirements. This workshop addresses these challenges through a comprehensive exploration of advanced thermal characterization, materials innovation, and holistic design methodologies that span from fundamental materials science to industrial-scale implementation. The program brings together leading researchers, and industry practitioners to present breakthrough approaches that are reshaping thermal management across the RF and microwave ecosystem. The technical foundation begins with the innovations in wide-bandgap materials presented by Prof. Srabanti Chowdhury of Stanford University, whose pioneering work on ultra-wide bandgap materials demonstrates how diamond integration with Beta-Gallium Oxide enables unprecedented reduction in thermal boundary resistance while maintaining RF performance. These materials advances provide the essential building blocks for next-generation thermal management solutions, particularly in high-power RF applications where conventional thermal interface materials reach fundamental limitations. Oscar D. Restrepo offers industrial thermal modeling and characterization perspectives from GlobalFoundries, where a unique combination of theoretical expertise in phonon transport and practical TCAD thermal simulation experience bridges fundamental physics with manufacturing-scale implementation. His work spans from first-principles calculations of defect formation energies to real-world thermal assessments across advanced technology nodes, including 22FDX and 12LP platforms. Building upon materials foundations, the workshop explores state-of-the-art thermal characterization techniques through both academic research and commercial implementation. Advanced thermoreflectance imaging, POSH-TDTR technology, and emerging measurement approaches demonstrate how nanosecond temporal resolution combined with submicron spatial accuracy reveals previously inaccessible thermal phenomena in operating RF devices. These characterization advances enable predictive thermal design that was previously impossible with conventional measurement techniques. Standards and validation methodologies receive dedicated attention through participation by the National Institute of Standards and Technology (NIST), which presents traceable thermal measurement techniques and validation protocols essential for industry adoption. NIST's gate resistance thermometry methods and RF power metering standards provide the measurement foundation necessary for reliable thermal characterization across different technology platforms. The workshop culminates in a holistic design philosophy that integrates materials innovation, advanced characterization, and system-level optimization. Live demonstrations showcase how this integrated approach enables thermal-electromagnetic co-design, abandoning traditional component-level optimization in favor of system-wide performance optimization. Real-world case studies span from mm-wave antenna-in-package modules to high-power GaN amplifiers, illustrating a direct correlation between materials

properties, thermal imaging data, and system performance. Interactive sessions throughout the workshop foster direct dialogue between materials researchers, device designers, and manufacturing engineers. These discussions address practical implementation challenges while exploring emerging opportunities that could reshape thermal management approaches over the next decade. The format emphasizes knowledge transfer and collaborative problem-solving rather than traditional presentation-only formats.

Speakers:

1. "Wide-Bandgap Material Characterization for Next-Generation RF Power Electronics", **Srabanti Chowdhury**, *Stanford University*
2. "Transient Thermal Dynamics in RF Wide Bandgap Semiconductors", **Georges Pavlidis**, *University of Connecticut*
3. "Thermal Modeling and Characterization Across Advanced Semiconductor Technologies", **Oscar D. Restrepo**, *GlobalFoundries*
4. "Self-Heating Characterization and Mitigation in Advanced RF Transistor Technologies", **Jean-Pierre Raskin**, *UCLouvain*
5. "Thermal Management Research Advances to Enable Next Generation RF Devices and Systems", **Yogendra Joshi**, *DARPA*
6. "Thermal Imaging Solutions to Address Emerging Thermal Challenges of Advanced Devices and 3DHI Packaging Techniques", **Mo Shakouri**, *Microsanj*

Networking Events

SUNDAY, 7 June 2026

RFIC Welcoming Reception and Symposium Showcase
19:30–21:00
Westin Boston Seaport District, Grand Ballroom

The RFIC Reception invites attendees to an engaging evening of social networking and technical exchange, supported by the RFIC 2026 sponsors. Complimentary drinks and refreshments will be served as you explore highlights from the industry showcase and student paper finalists. This interactive setting allows for close-up discussions with authors demonstrating their work in a lab-like environment. RFIC registration or RFIC Reception Ticket is required for entry.

MONDAY, 8 June 2026

IMS Welcome Event
20:00–21:30
Prudential Center, View Boston

IMS'26 starts with a welcome event on Monday for all attendees, which will be hosted at the View Boston atop the Prudential Center following the IMS'26 Joint RFSA/RFTT Plenary Session.

TUESDAY, 9 June 2026

Student-Industry-Academia RFIChat
"Catching the Next Wave: How to Spot the Next Big Thing and Make the Jump"
17:-00–19:30
MCEC, Room 259AB

This social event on Tuesday is open to all registrants! This panel discussion is designed to help students and professionals navigate career opportunities in the RF field. The session will conclude with networking and complimentary food/beverages for everyone.

Amateur (HAM) Radio Reception
18:00–20:30
Westin Boston Seaport District, Commonwealth Room

All radio amateurs and other interested IMS participants are cordially invited to the event. The reception schedule is as follows:

18:00–18:30: A social mixer with provided food and drinks. Bring your QSL card to exchange.

18:30–19:30: Invited presentation on the new FlexRadio Aurora by Tony Brock-Fisher K1KP.

19:30–20:30: Special topic booths on the many facets of amateur radio and information on how you can "get on the air" (including getting your FCC amateur radio license).

Women in Microwaves (WIM) Reception
18:30–20:30
Boston Institute of Contemporary Art (ICA)

This event welcomes all members of IMS to promote collaboration, with a spotlight on the work of female RF engineers and researchers. The reception will include light refreshments of hors d'oeuvres and drinks. Participates will network and have the opportunity to engage in a scavenger hunt-style game to wins prizes!

Networking Events (continued)

Young Professionals (YP's) Reception
18:30–20:30
Fight Club Darts

This year's YP social event will feature an exciting retro video arcade game tournament, with priority registration for YPs attending the conference. The tournament will include classic games such as Super Mario, Street Fighter, NBA Jam, and Guitar Hero, evoking nostalgia while offering a fun and engaging environment for social networking. Scheduled during conference breaks, this lively event provides an opportunity to relax, showcase gaming skills, and enjoy light refreshments to stay energized. Beyond the competition, attendees can connect, collaborate, and build camaraderie in a relaxed setting. Prizes will be awarded to the top three participants for each game.

MTT-S Journals Reception & Poster Session
19:00–21:00
Westin Boston Seaport District, Grand Ballroom, Section A

Don't miss this opportunity to learn more about our publications and to interact with our Editors and Board members. Get your questions answered and give your feedback — positive and negative — directly to those who handle your manuscripts or who are constantly asking for more and more of your precious time to do reviews! We can't wait to see you for the first time, or to meet you again in Boston at this flagship event.

The event will require a reserved ticket. The cost of entry is the promise to do some reviewing for one or more of our sponsored journals over the coming 12 months. You can sign up for a ticket by using the link here:

https://app.smartsheet.com/b/form/019db00439e170a9bd3826e8ab41d9de

WEDNESDAY, 10 June 2026

Industry-Hosted Reception
17:00–18:00
MCEC, IMS Exhibit Floor

Ride the Wave of Excitement to the Industry Hosted Reception on the IMS Exhibit Floor! Indulge in delicious appetizers and beverages with colleagues, friends, and exhibitors.

MTT-S Awards Banquet
18:30–20:00
Westin Boston Seaport District, Grand Ballroom

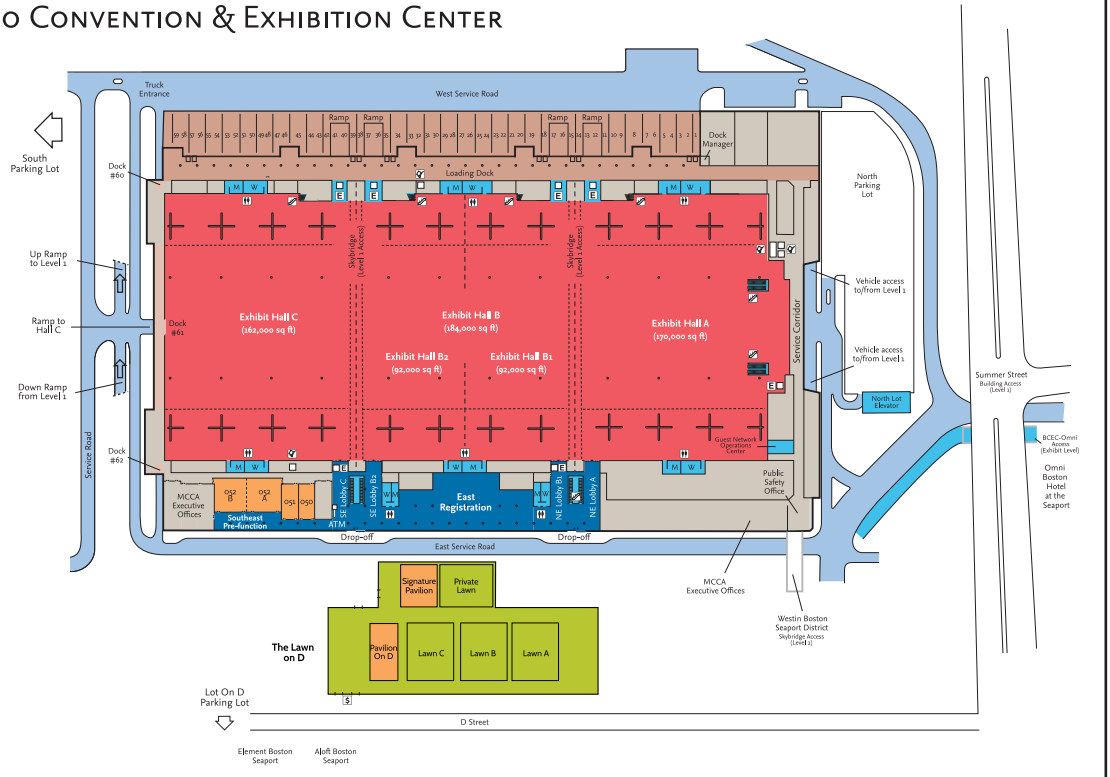
Join us in celebrating this years MTT-S Award Winners, IEEE Fellows and other honored guests! The MTT-S Awards Banquet will include fine dining, an awards presentation, and excellent entertainment. Ticket is required for entry.

Thomas M. Menino Convention & Exhibition Center

Exhibit Level

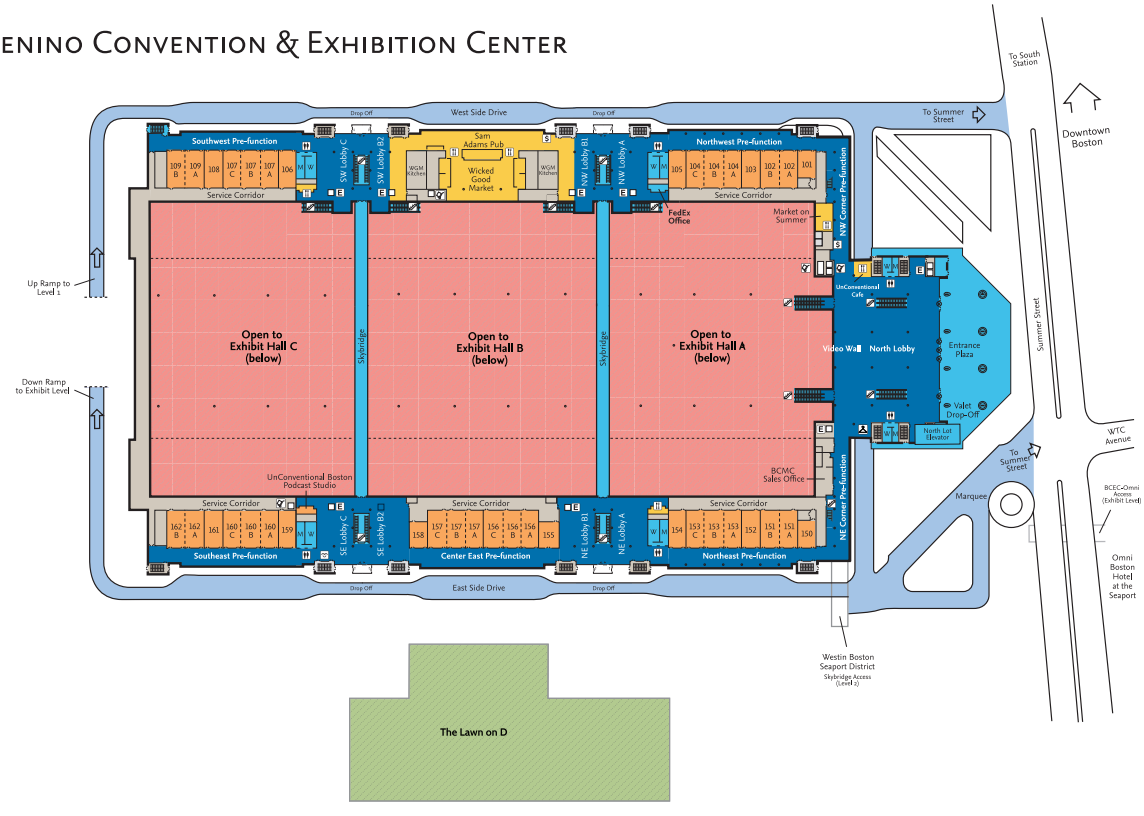
- Exhibit Space
- Meeting Rooms
- Ballroom
- The Lawn on D
- Lobby & Pre-function
- Public Use
- Ring Road
- Non-Public Access
- Loading Dock Pre-Feb Area & Loading Dock Covered Truck Access
- Food Services

- Elevator
- Freight
- Escalator
- Restrooms
- Permanent Concessions
- Suggested Coat Check
- Stairs



Thomas M. Menino Convention & Exhibition Center

Meeting Level 1

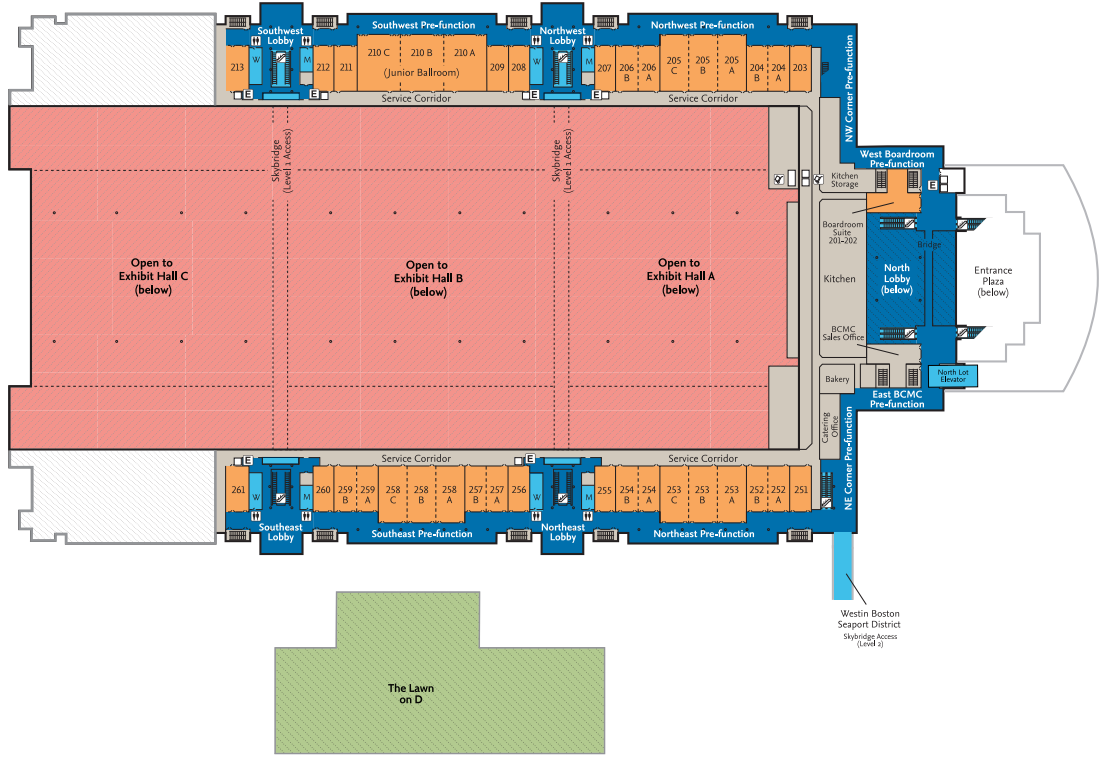


Thomas M. Menino Convention & Exhibition Center

Meeting Level 2

- Exhibit Space
- Meeting Rooms
- Ballroom
- The Lawn on D
- Lobby & Pre-function
- Public Use
- Ring Road
- Non-Public Access
- Loading Dock Pre-Feb Area & Loading Dock Covered Truck Access
- Food Services

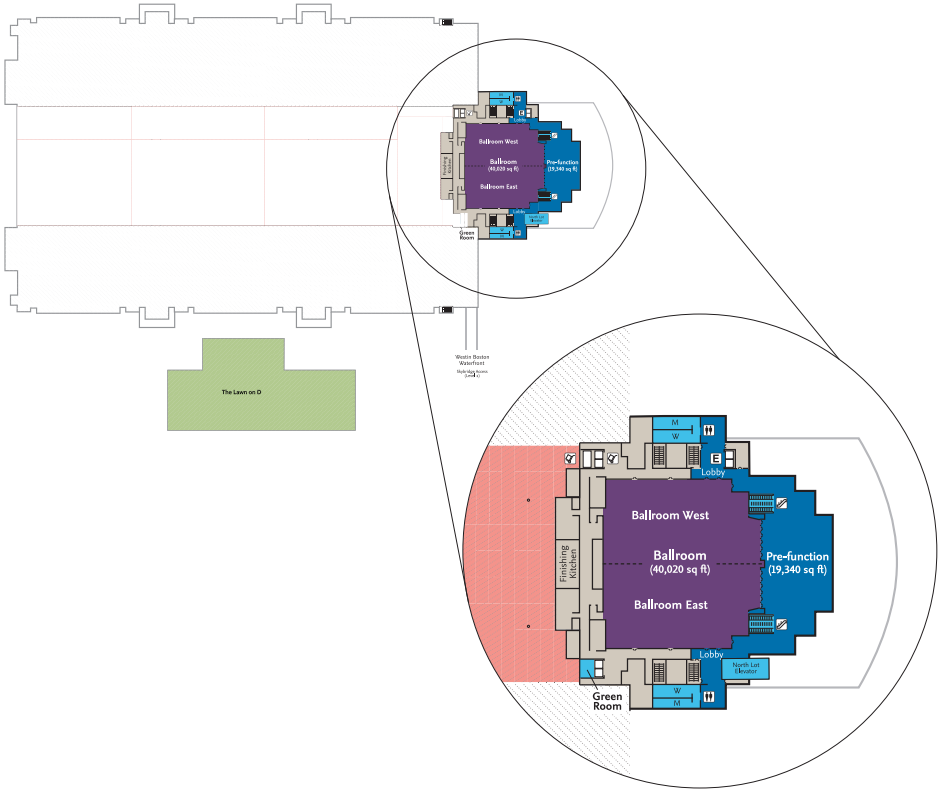
- E Elevator
- Freight
- Escalator
- Restrooms
- Permanent Concessions
- Suggested Coat Check
- Stairs



Thomas M. Menino Convention & Exhibition Center

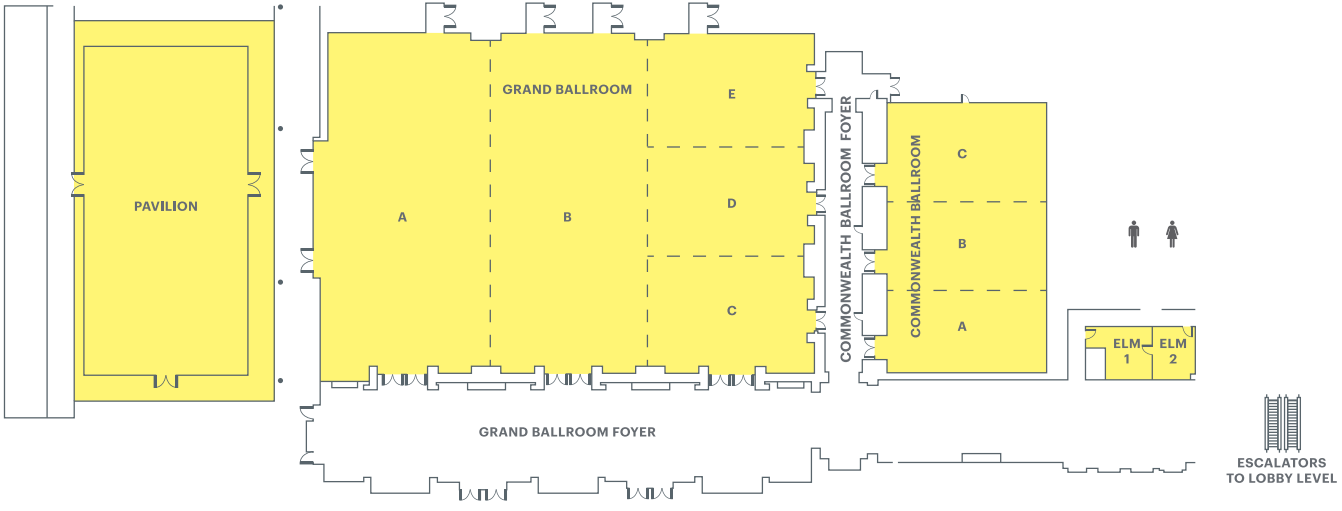
Ballroom Level 3

- Exhibit Space
- Meeting Rooms
- Ballroom
- The Lawn on D
- Lobby & Pre-function
- Public Use
- Ring Road
- Non-Public Access
- Loading Dock Pre-Feb Area & Loading Dock Covered Truck Access
- Food Services
- Elevator
- Freight
- Escalator
- Restrooms
- Permanent Concessions
- Suggested Coat Check
- Stairs



THE WESTIN
BOSTON SEAPORT DISTRICT

Concourse Level



NOTES

IEEE
445 Hoes Lane
Piscataway, NJ 08854, USA

2026 RFIC Symposium
Boston, Massachusetts, USA
7–9 June 2026

RFIC PROGRAM