IMS2025 Student Design Competition

Power Amplifier Linearization through Digital Predistortion (DPD)

Introduction

Digital predistortion (DPD) linearization, after about 25 years development, has become the most popular distortion cancellation method of choice to relax the linearity-efficiency compromise of wireless systems.

Modern orthogonal frequency division multiplex (OFDM) spectrally efficient communication signals present high peak-to-average power ratio (PAPR). This constraint forces the system to operate the power amplifier (PA) at a large output power back-off in order to guarantee the required linearity level at the antenna port, leading to a serious degradation of average power efficiency. To minimize power dissipation, highly efficient amplification architectures based on the dynamic load or dynamic supply modulation have been proposed in the literature. PA architectures based on active load modulation, such as the load-modulated balanced amplifier (LMBA), are based on the nonlinear interaction between multiple transistors with the objective of enhancing the overall average efficiency when handling high PAPR modulated signals. The degrees of freedom offered by the additional RF inputs can be exploited to optimize the performance in terms of some of the most relevant key performance indicators (KPI) in power amplification: gain over bandwidth, linearity and, average efficiency. The LMBA requires the use of digital signal processing to generate the load modulated control signal to maximize power efficiency, as well as digital predistortion (DPD) linearization techniques to guarantee the stringent linearity requirements of today's systems, especially with the increasing signal bandwidth.

The goal for this Student Design Competition (SDC) is to maximize the total drain efficiency of a dual-input LMBA while meeting both in-band and out-of-band linearity specifications when considering 5G NR wideband modulated signals.

Following the previous editions of the DPD Student Design Competition, a remote-controlled measurement setup (WebLab) consisting of the PA to be linearized and proper instrumentation will be made available for the competitors prior to IMS. Measurements can then be performed remotely using this virtual laboratory setup in order for the competitors to develop and tune their DPD algorithms.

Design specifications and rules

The DPD-Competition is open to teams of undergraduate and/or graduate students that are registered at a university or other educational institution. The maximum number of participants per team is three. Participants cannot be associated with more than one team. Students currently affiliated with the Universitat Politècnica de Catalunya, UPC- Barcelona Tech., Spain, cannot participate in the competition.

At least one member from each team must be present at the competition held during the IMS-2025. After the registration period ends, a time-table for the competition day will be made available, with the schedule of the 15 minutes slots of the participating teams. If no

team member is present at the competition site within its slot, then the team may be considered as absent.

The MATLAB scripts required by each team to implement and tune their DPD algorithm at the competition must be brought on a USB memory stick. At the IMS-2025 competition, the hardware setup will be controlled by a PC to which the teams will have access during their 15 minutes time slot. It will not be possible for participants to connect their own computers to the hardware setup during the competition. The scripts and files brought by the teams will not be stored, but deleted from the PC after the participation of each team.

Participants must register to the IMS Student Design Competition according to the rules posted on the IMS-2025 homepage. **At the same time as the registration to IMS-2025 is made, the competitors must also register with the organizers of the competition. This is done by sending an e-mail containing the name of the team members and their contact details (e-mail preferred) to pere.lluis.gilabert@upc.edu and to gabriel.montoro@upc.edu with the subject line "IMS SDC: Registration DPD-linearization competition" no later than the official deadline announced on the IMS-2025 SDC homepage.**

In accordance with IMS general rules, it is required that the designed algorithms are principally the work of the students.

Please also see the general IMS student design competition rules on the IMS-2025 SDC homepage.

Evaluation process

The objective of this SDC is to design a DPD algorithm appropriate to the linearization of a given dual-input LMBA. The complete transmitter chain to be linearized comprises the following devices and instrumentation:

- Dual-input LMBA DUT.
- Wideband direct RF/uW arbitrary waveform generator (AWG) or Wideband I/Q AWG and modulator (depending on the specific instrumentation made available by the equipment sponsor).
- Signal analyzer.

The participants will be able to remotely (via the WWW) upload the main and control signals to the LMBA after DPD. The PA response (also, the baseband envelope signal) will be retrieved by the signal analyzer. The scoring results will be also provided. The participants' DPD algorithms will be run off-line, similarly to the earlier editions of the DPD-Competition, and a realization of the target input signal used in the competition will be made available to the participating teams. A realistic OFDM telecommunications signal will be used as input, which will cover a significant part of the PA's available bandwidth.

Through a dedicated web site, the participating students will be able to test their algorithms with the hardware setup, by remotely uploading the both input signals after DPD, and capturing the respective output signals. Both the web site and the input signal format to be considered in the DPD-Competition will be made available well in advance to the competition.

In the DPD-Competition, to be held in the IMS-2025, the same hardware test setup (or other samples of the same devices) will be made available to the participating students, where they will be able to tune their DPD algorithms and upload their predistorted and supply

signals. Each team will have a period of 15 minutes to tune its DPD model. When ready (or at the end of that 15 minutes period) the target input signal will be given to the team and its DPD will generate the predistorted and bias supply signals, which will be uploaded to the signal generator and supply modulator. At that moment, the jury will measure (and register) the performance metrics used to compute the overall score achieved by the team.

Scoring

The DPD-Competition goal is to maximize a numerical score, which is used to rank each participating students' team. It will be calculated by a formula, defined long before the competition (and made available to the teams), which increases with the total efficiency of the LMBA, although restricted to a specific spectral emission mask and weighted normalized mean square error (NMSE). The computational complexity of the DPD algorithm will also be measured in terms of minimum number of required resources, for example particularizing in the number of coefficients used by the DPD algorithm. The exact score formula will be designed and adjusted based on our assessment of the device to be linearized

Name and number of supporting MTT-S Technical Committee

TC-15 RF/Mixed-Signal Integrated Circuits and Signal Processing Committee

TC-12 Microwave High-Power Techniques Committee

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Equipment information

Hermann Boss from Rohde-Schwarz will take care of providing the signal generation and measurement instruments required for the competition. Tentatively, it will consist in a vector signal generator (R&S SMW200A) and a spectrum signal analyzer (FSW8).